Gate decorated Field Effect Transistors for high sensitivity pH sensing

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Abstract

We present a micro/nano-machining process to introduce nanostructured poly-silicon layer on the gate region of the pH-sensitive field effect transistors. Decoration of the gate of the field effect transistors by nanostructures plays an important role to improve the sensitivity of the pH-sensitive FETs. Electron beam lithography was exploited to realize the poly-Si nanopillars on the gate surface. Comparison between different micro and nanostructures demonstrates the potential of nanopillars to be utilized on the gate of this device rather than micro-conical structures (different size and shapes) and vertically carbon nanotubes. A high sensitivity of 500 mV/pH has been achieved, through the incorporation of silicon based nanopillars.

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Keywords: micro/nano-machining process, poly-Si nanostructure, pH-sensitive FET, nanopillar.

1. Introduction

Since the discovery of ion sensitive field effect transistors in 1970, they have found great applications in pH measurement units and bio-sensors [1]. The application of pH-FETs in bio-sensing has been investigated during the past 30 years [2-5]. Fast and accurate response as well as low cost and compatibility with commercial IC processes make them favorable for disposable biosensors [6-9]. A chemically sensitive insulating layer is replaced for the gate of a metal oxide semiconductor field effect transistor (MOSFET) to form a conventional ISFET [10]. The surface perturbations caused by variations of charges at the interface shift the threshold voltage based on Nernst law and modulate the drain-source current in the channel of ISFET. The most common sensitive layer used in ISFETs as gate insulator is SiO_2 but other gate insulators like Si_3N_4, Al_2O_3 and V_2O_5 are used as sensitive gate insulator on top of the SiO_2 layer to enhance the sensitivity of ISFETs [3]. Nevertheless, these oxide insulating layers could not help to exceed beyond the Nernstian limit of 59 mV/pH.

The H+ sensitive FET is one of the most important ISFETs used as biosensor. In most bio-sensing applications, the pH of target analyte is monitored to detect the signal transduced by ISFET due to chemical reactions on the gate surface functionalized by biological recognition elements. In order to detect chemical reactions in the low concentration volume of analyte, it is necessary to have an ISFET with higher sensitivity. As an example in the process of DNA synthesis, during lining up of each base-pair one H^+ is released. High sensitivity ISFET is required to detect the generation of one H^+ ion [11]. Double-gate FET (DGFET), floating-gate FET (FGFET) and extended-gate FET (EGFET) are the most important devices proposed to enhance the sensitivity of ISFETs [12].

On the other hand, nanostructured semiconductors have emerged as promising elements to be utilized in functional devices such as sensors and transistors. In particular, silicon nanowires exhibit excellent electronic properties and large surface-to-volume ratios as

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well as their compatibility with conventional silicon technology. They could be readily synthesized via bottom-up or top-down processes. Although the top-down process is attractive owing to its possibility to preserve the desired designing organizations, the evolution of ultra-small features (at deep nano-metric scale) allows the interaction of electrolyte and solid at a so-called Debye length level.

In this work, we have fabricated highly doped poly-Si micro-conic and micro-pillar structures over the gate area with high density and uniformity for pH sensing. A top-down (DRIE) technique based on photolithography was used to define n-doped poly-Si micro-conic arrays. Furthermore, we have grown multiwall CNTs around the micro-conic structures to compare pH sensitivity of these transistors before and after CNT growth. We observe that poly-Si nanopillars dramatically enhance the sensitivity of the compared to the other mentioned structures. The promising sensitivity of poly-Si nanopillars on the gate surface besides biocompatibility and ease of bio-target immobilization makes them desirable for bio-sensing applications like DNA sensing.

2. Fabrication Details

The n-channel transistors were fabricated on p-type silicon (<100> orientation) wafers. Thermally grown silicon dioxide was used as the gate insulator through the dry oxidation furnace. The thickness of SiO_2 layer is about 95 nm. A low pressure chemical vapor deposition (LPCVD) method was utilized to deposit 700 nm poly-Si as the gate region with a mixture of SiH_4 and H_2 (30/75 sccm, respectively). The source and drain regions were introduced through the diffusion of phosphorous in predefined patterned area using diffusion furnace.

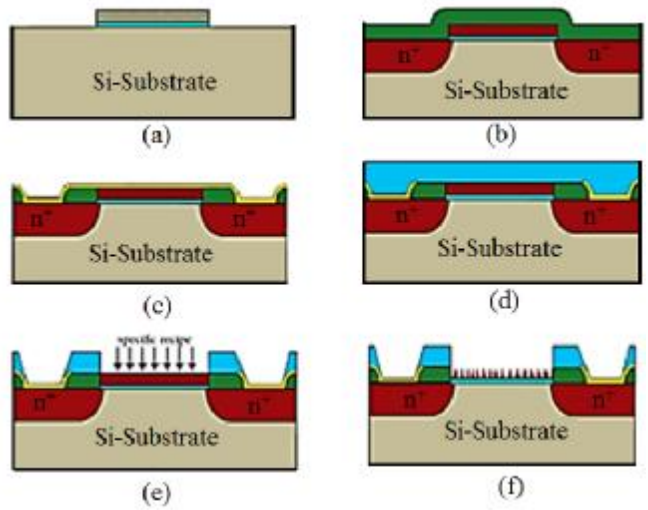

Figure 1: The schematic images depicting the fabrication process of pH-sensitive FET compatible with a standard process. Parts (a) and (b) show the formation of transistor. The formation of source/drain windows coated with metal is depicted in (c) and (d). Finally, in (e) and (f) the highly porous gate region is realized by means of reactive ion etching.

Poly-Si layer was also doped to act as the electrode for gate. The channel length and width are 50 and 100 µm respectively. RF-PECVD deposited SiO_xN_y layer was used to passivate the whole surface of the ISFET except opening area to gate region. Packaging of the sensor was conducted using thick negative photoresist (SU8) where the gate region and gold contacts of source and drain were opened to contact with electrolyte and V_{DS} connections, respectively. The fabrication process is schematically depicted in Figure 1. In addition, SENTEK R1/Ag-AgCl/2MM was employed as a reference electrode with a bias voltage of 0-5 V. A Hitachi S-4160 was used to investigate the morphology of the structures mentioned in this paper. Figure 2 shows cross sectional view of scanning electron microscope (SEM) image of 700 nm poly-Si layer deposited on 95 nm SiO_2/Si.

A deep reactive ion etching was used to introduce the nanostructures onto the poly-Si layer. A thin layer of Cr (10 nm) was used as a metal hard mask in the vertical etching process. A textured poly-Si layer was made by a sequential reactive ion etching process consisting of sequential etching and passivation mechanism. During the etching step, SF_6 gas enters into the chamber at the presence of plasma operated at

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13.56 MHz to vertically etch poly-Si layer. In the passivation step, the poly-Si trench walls are protected by given flows of H_2 and/or O_2 and a trace value of SF_6. The formation of ultra-small features is feasible through controlling the gas flows and the plasma power and duration.

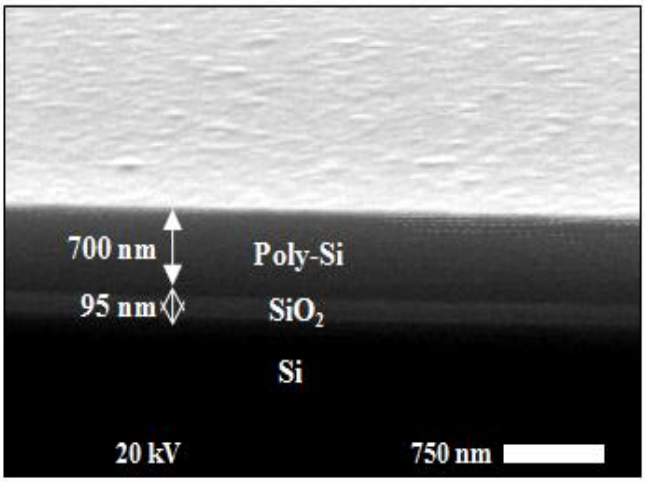

Figure 2: The SEM image of 700 nm poly-Si layer deposited on SiO_2/Si substrates by LPCVD unit.

Table 1 shows the different micromachining steps to arrive at vertical nanostructures in more detail. Steps 1-1 and 1-2 are used to make a suitable passivation layer while during the last step (1-3), the etching is predominant. An electrical parameter analyzer was utilized to measure the I-V characteristics of the pH-sensitive FET in different pH values.

Table 1: Sequential procedure in DRIE system to obtain vertical features

Process step	Gas type	Flow (sccm)	Power (W)	Time (S)
1-1	O_2, SF_6, H_2	0, 5, 260	240	60
1-2	O_2, SF_6, H_2	90, 0, 0	110	50
1-3	O_2, SF_6, H_2	0, 110, 23	150	7

3. Results and discussions:

To investigate the structures and dimensions of poly-Si elements on the gate surface, highly doped poly-Si nanopillars were fabricated on the gate surface to introduce a nanopillar-decorated pH-sensitive FET. The schematic of the highly ordered nanopillars on the gate of the device is depicted in Figure 3.

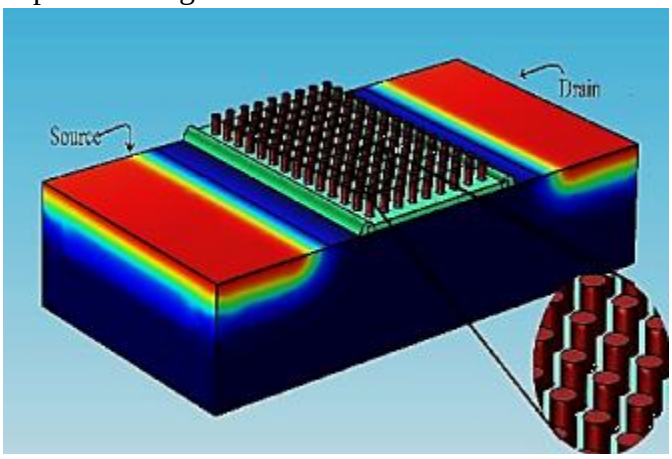

Figure 3: The schematic of the pH-sensitive FET immersed in the solution to measure the pH value, where poly-Si nanopillars were fabricated on the gate of the device through the vertical etching and electron beam lithography. Inset shows magnified image of poly-Si nanopillars. Apart from such vertical features, the formation of small nano-structures is feasible on top of such vertical features.

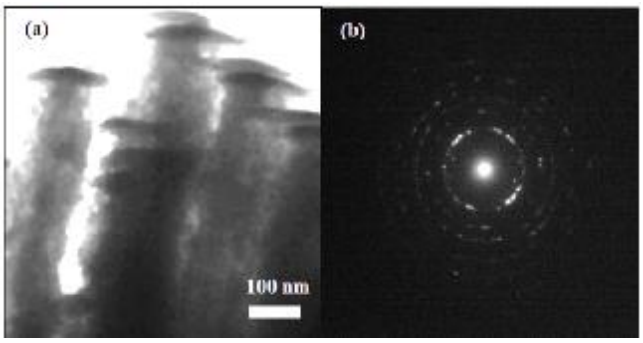

Figure 4: (a) TEM of the poly-Si nano-rods before using Ni-etchant to remove hard masks. (b) SAED of the poly-Si nanopillars which clearly demonstrates the poly crystallinity of the nanopillars.

A Philips CM30 transmission electron microscopy was exploited to investigate the structure of poly-Si nanopillars. A TEM image of the poly-Si nanopillars is presented in Figure 4 (a). Selected area diffraction pattern demonstrates the poly crystallinity of the nanopillars fabricated on the device gate. The edges of the nano-pillars show the evolution of ultra-small features at deep nano-metric scales.

Electron beam lithography was employed to define poly-Si nanopillars on the gate of the device. We have used PMMA as electron-sensitive layer along with thin layer of Ni (6 nm) deposited by electron beam evaporation system as a hard

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mask. Afterward, DRIE was exploited to vertically etch the poly-Si layer and introduce vertically aligned poly-Si nanopillars. Nano-patterns (less than 150 nm) were realized through the electron beam lithography (Figure 5 (a)). After Ni deposition, the PMMA layer was removed using a lift-off process with acetone solvent, which was not successful attempt (Figure 5 (b)). By a combination of acetone and Tetrahydrofuran (THF) solvent we could arrive at complete lift-off and subsequently nano-pillars as seen in parts (c) and (d) of this figure.

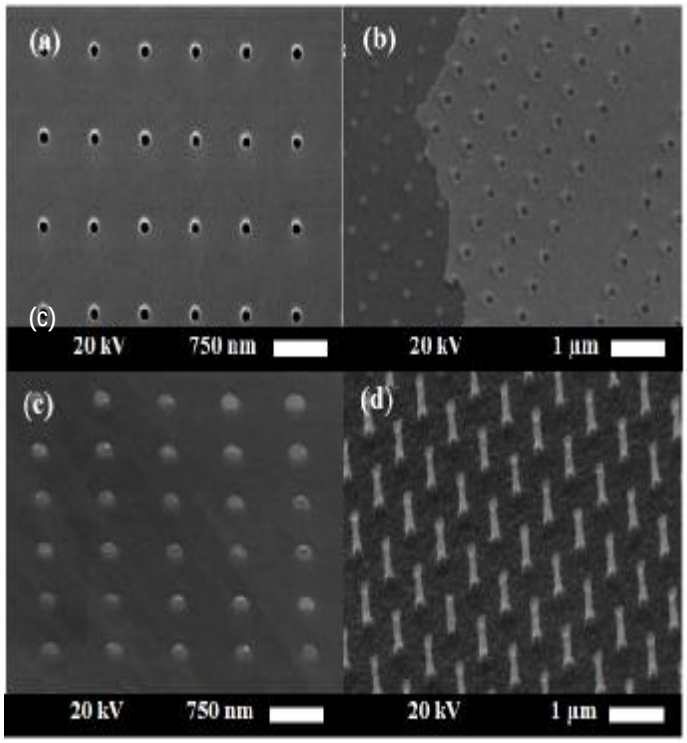

Figure 5: Fabrication process of poly-Si nanopillars. (a) Electron beam lithography of PMMA on the gate surface. (b) Ni deposition on PMMA and lift-off with acetone. As seen the lift-off is not successful with acetone. (c) As an alternative, THF is a strong solvent and it was used as a remover to completely lift-off PMMA. (d) Ni dots were employed as hard mask required for subsequent vertical etching process.

4. Electrical Characterizations:

The electrical characterizations of the poly-Si nanopillar FET were carried out using a Keithley parameter analyzer unit. All the electrical measurements have been conducted at room temperature and under ambient conditions. The results presented in Figure 6, demonstrate the high sensitivity of the fabricated device to pH variations in the solution. Different parts in this figure correspond to various values of pH, ranging from 4 to 9 (acidic to basic solutions). The monotonic drop in the device drain current represents the shift in the threshold voltage at different values of pH. Part (d) in this figure collects all three cases at a given reference electrode voltage of 5V to make an easy comparison.

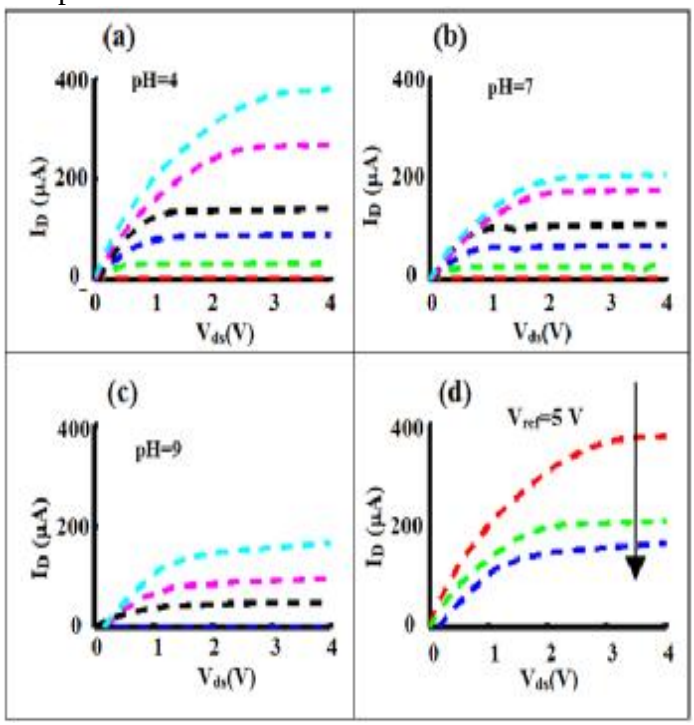

Figure 6: The I_D-V_D characteristics of the poly-Si nanopillar pH-sensitive FET; V_{REF} was set to 0, 1, 2, 3, 4, and 5 V, respectively. (a) pH=4, (b) pH=7, (c) pH=9, and (d) The I_D-V_D characteristics of the device at V_{REF}=5 V for different pH values from 4 to 9.

The transfer characteristic of the device (I_D-V_D) is presented in Figure 7, clearly showing high sensitivity of the porous poly-Si nanopillars in contrast with microstructures or carbon nanotubes. A high sensitivity up to 500 mV/pH is reported as a record value for ISFET devices. Part (a) in this figure shows the SEM image of the fabricated transistor where the active region is magnified and shown in part (b). The formation of highly ordered rods (pillars) is evident from this figure. The suggested mechanism of the site-binding is also shown in part (c) where various species such as $[O]^-$, $[OH_2]^+$ and [OH] are attached on the effective surfaces of the devices both on the walls as well as the bottom surfaces between neighboring rods. Such charges are responsible for the formation of Helmholtz double layer and

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consequently for the shift in the threshold voltage. More elaboration on the physical and chemical modeling of the device is underway.

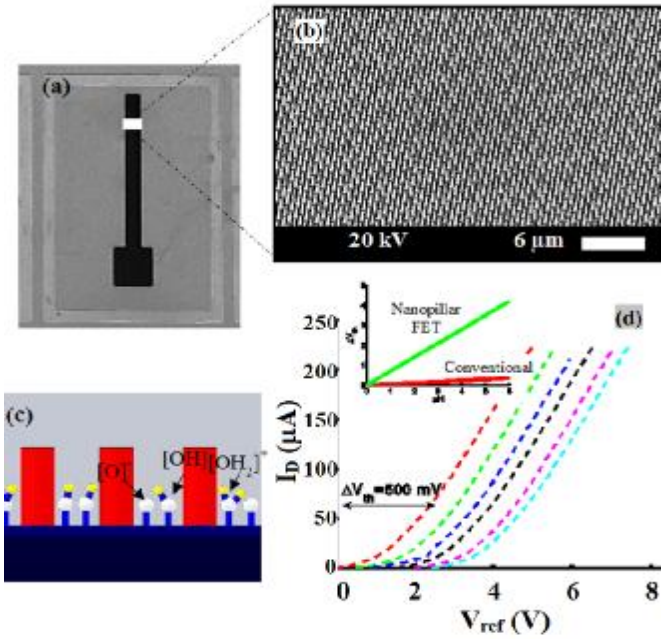

Figure 7: Poly-Si nanopillar arrays uniformly created in the area of 100 µm×50 µm to enhance the sensitivity of the device. (a) SEM image of the Poly-Si gate pattern. (b) SEM image of uniform nanopillar array on the gate. (c) Schematic of the surface sites in the space between two nanopillars, [OH], $[OH_2]^+$ and $[O]^-$. (d) Transfer characteristic of the device measured at the solution while pH varying from 4 to 9; Inset shows the difference of nano-structured versus the planar ISFET device.

Apart from poly-silicon nano-pillars, we have grown carbon nanotubes on the previously micro-conical structures. The microconical features are obtained using mask undercut during the RIE process. The masks for this examination have been set at 3µm dimeter. Figure 8 collects several SEM images of such configuration prior to the growth of CNTs (parts (a) to (c)). The carbon nanotubes (CNT) were grown on the gate of the device through the Ni deposition and subsequent direct-current plasma enhanced CVD (dc-PECVD) method. The growth occurs at a chamber temperature of 680 °C and in the presence mixture of gases including acetylene and hydrogen with flows of 7 and 20 sccm, respectively. Figure (8.e) depicts the SEM image of vertical CNTs grown on the gate surface. Larger poly-Si islands are visible in this figure. The corresponding I_D-V_{REF} characteristics of this configuration show a non-linear behavior compared to the planar or micro-conic polysilicon gate. In certain regions, one can observe a higher threshold voltage shift compared which could be due to the presence of more surface sites and consequently, more interaction with sensing layer. Comparing the results of this investigation with the nano-pillar structures, one can conclude that the nano-pillar decorated gate is more suitable and more linear for pH-sensing.

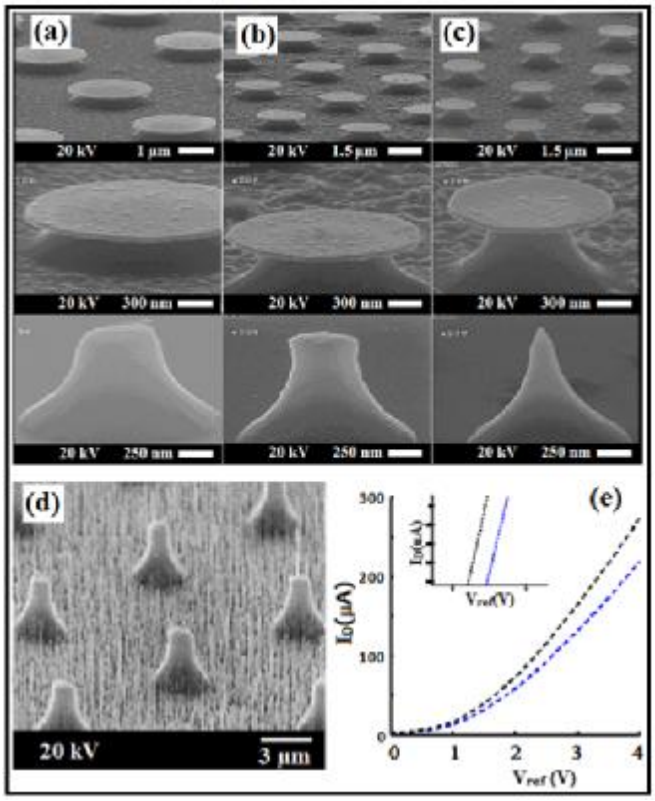

Figure 8: (a)-(b) and (c) The SEM images of the formation of micro-conical structures on polysilicon layers. Larger masks are used to allow for a controllable undercut. (d) The SEM image of CNT incorporated poly-Si gate. (e) I_D-V_{REF} characteristics clearly show the higher threshold voltage shift of this structure than poly-Si micro-conic structures when pH of the solution varies from 3 to 5.

Table 2 shows the comparison between our structure and different ISFET topologies.

Table 2: Comparison Table of different ISFET topologies.

	Conv. ISFETs Bergveld et al	D. Gate ISFETs (Go et al.)	D. Gate NWFET Knop. et al	D. Gate ZnO-NWFET Zafar et al.)	This Work
Sens. (mV/pH)	<57	60-240	220	2250	500
Using Dual Gate	No	Yes	Yes	Yes	No

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5. Conclusion

In this paper a novel method based on sequential reactive ion etching process was developed to fabricate nano-porous poly-Si layers as the gate region of ISFET to improve its sensitivity in contrast with the conventional ISFETs. The evolution of nano-textured features on the silicon pillars enhances the nonlinearity of ISFET response compared to planar gate ISFETs. Additionally, the gate-engineered surfaces specially on the gate of the ISFET makes it desirable for ion sensing like H^+ detection in the solution while containing DNA molecules. We believe this ISFET is a promising candidate for low concentration of DNA detection and DNA sequencing.

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