Short-Switch Fault Ride-Through andPost-Fault Reconfiguration Strategy for a Static Synchronous Series Compensator Based on Cascaded H-Bridge Multilevel Converter

Amir Sepehr[1], Mehdi Saradarzadeh[2*], Shahrokh Farhangi[1]

***Abstract*— The cascaded H-bridge (CHB) converter is one of the viable options for large-scale power conversion. Owing to the increased number of components involved in this topology, converter reliability and fault-tolerant control are important issues. This paper proposes a new short-switch fault protection scheme and a post-fault modulation (PFM) strategy to keep the performance of a CHB converter in a static synchronous series compensator (SSSC) application. The SSSC is a series converter to the transmission line, which controls the power flow in the line. Acting as a series converter, any abnormal action of SSSC can affect the whole line reliability. So following the fast fault detections and protections, remedial actions have to be considered to extend normal operation of the SSSC and, in some cases, derate the system to prevent unexpected shutdowns. The new method of short switch fault protection can eliminate the fault in the proper time, while the novel proposed PFM strategy guarantee the continuation of converter operation. This method is based on the application of increasing dc bus utilization techniques in conjunction with the phase shifted pulse width modulation method, which generates the balanced grid currents. Take the advantages of this method; the converter is able to control the transmission line power flow with the remaining healthy H-bridges. Simulation results validate the effectiveness of the proposed method.**

***Index Terms*—: cascaded H-bridge, multilevel converter, post-fault reconfiguration, short-switch fault, static synchronous series compensator**.

Nomenclature

U_{PWMa}, U_{PWMb}, U_{PWMc}	Phase voltage references for phases A, B, and C.
φ_{PSa}, φ_{PSb}, φ_{PSc}	Carriers' phase shifts for phases A, B, and C.
N	Numbers of HB cells per phase.
A_m	Modulation index before fault occurrence.
A_{m3}	Third-harmonic injection modulation index
$A_m^{boundary}$	Modulation index boundary value before fault occurrence.
A_m^{new}	Damaged phase post-fault modulation index.

I. Introduction

Enhancing high-power converters reliability is of paramount importance, especially in the multilevel converters, where generally a large number of power switching devices are used and each of these devices may be considered as a potential failure point. Furthermore, the possibility of fault occurrence is much larger than the conventional two-level voltage-source converters. Faults in the power semiconductor devices will cause a power converter to operate far away from its setting point and this abnormal operation cannot be managed by a feedback controller. So obviously, it is essential to detect and locate the fault within a short time after the occurrence, and remove it. The underlying reason of this action is that the fault may distort the voltage and current, and even destroy the converter. The Static Synchronous Series Compensator (SSSC), a solid-state voltage source inverter coupled with a transformer, can be connected in series with a transmission line, and control the electric power flow [1]. Multilevel converters are preferred solutions for reasonable to consider each phase as

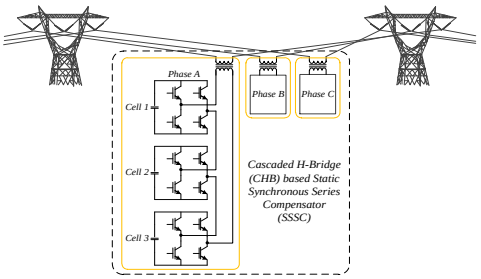

Figure 1. Cascaded H-bridge multilevel converter as an SSSC

Manuscript received April 13, 2016; accepted October 18, 2016

[1]MSc Student in Electrical Engineering, Power Electronics Branch, School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Tehran, Iran.

[2]Assistance Professor of Electrical and computer Engineering Department , Jundi-Shapur University of Technology, Dezful, Iran. Email: saradar@jsu.ac.ir

[3] Full Professor of Electrical Engineering, School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Tehran, Iran.

an independentpart, as shown in Figure 1. Since there is no auxiliary source to supply the dc buses and inject active power to the line, the SSSC is able to control only one of the active or reactive components of the power flow in the line at the same time [2].

In addition, reliability and durability are the most important challenges for an SSSC, where generally delivering a large amount of power depends on its proper operation [2, 3].

Following early stage fault detections in high-power converters, remedial actions can extend their normal operation and, in some cases, derate the system to prevent unexpected shutdowns. A remedial action typically contains a combination of hardware and software reconfigurations [4-6]. The conventional two-level inverters rely mainly on hardware reconfiguration, however, multilevel inverters demonstrate more capabilities to tolerate internal faults with a balanced combination of hardware and software reconfigurations [3-8].

Fault tolerant operation of the CHB converter in PV power plants when faults occur and unequal power is generated among the healthy bridges has been discussed in [3]. A modified Selective Harmonic Elimination (SHE) method in conjunction with Fundamental Phase Shift Compensation (FPSC) technique to generate balanced voltages and manipulate voltage harmonics at the same time in a CHB converter with a single faulty switch has been proposed in [4, 5]. The proposed Space Vector Modulation (SVM) technique uses an altered space vector diagram and a reshaped path for the rotation of the reference vector to generate phase-ground voltages with modified phase angles and different amplitudes [4, 5]. Moreover, artificial intelligent techniques such as fuzzy-logic and neural network have been applied in condition monitoring and fault diagnosis [6-8]. Topologies with fault-tolerant ability to detect one or more power H-bridge (HB) damaged cells has been proposed in [9], [10], which is based on the use of additional magnetic contactors in each power HB cell to bypass the faulty one. A comparison of features, cost, and limitations of fault-tolerant three-phase AC motor drive topologies has been investigated in [11]. A switch-based control method for operating the inverter with healthy switches in the faulty cell has been proposed in [12], and the maximum achievable output voltage of the inverter with faulty switches for the SVM technique has been calculated as well. However, this method is just suitable for SVM. Furthermore, a cell neural network classification method has been applied for fault diagnosis of a CHB in [13]. Meanwhile, the proposed fault diagnostic system requires about 150 ms to clear a short circuit fault. Moreover, a method to generate a balanced three-phase line-to-line voltage by phase-shifting and bypassing faulty power cells has been proposed in [14], this method is applicable for the ac drives but because of the separation of the phases in an SSSC, this method cannot be used in such a case. A reconfiguration system based on bidirectional electronic valves has been designed for Asymmetric three-phase CHB inverters in [15], but the shortcoming of this topology is that the HB cells are not interchangeable. N+1 redundancy strategy is another method that has been adapted for CHBs [16], but any redundancy strategy requires initializing the redundant cell and pre-charging the capacitors which are almost sophisticated steps in a faulty converter.

One can see from the concise literature survey is that the knowledge and information of fault behaviors in the multilevel converters is important to improve system design, protection, and fault-tolerant control. Thus far, limited research has focused on reconfiguration of the converter after fault occurrence without deployment of redundant devices. Conventional fault-tolerant methods can be classified as adding redundancy or using external circuits. These methods basically use hardware backup to improve the system reliability, which significantly increases the investment budget and adds the system complexity. On the contrary, modulation reconfiguration, which is actually a software redundancy, does not significantly increase the installation investment. Switching patterns and the modulation index of active cells of a faulty converter can be adjusted to maintain the operation under balanced load condition. Of course, the converter cannot be operated at full rated power, and the amount of reduction in capacity that can be tolerated, depends upon the application; however, in most cases a reduction in capacity is more preferable than a complete shutdown.

The main purpose of this paper is to provide a pragmatic approach to deal with short-switch fault in a CHB multilevel converter which can be used as an SSSC. This paper proposes a novel short-switch fault protection scheme and a PFM strategy to keep the performance of a CHB based SSSC. The proposed short-switch fault protection circuit is fast enough to save the healthy switches and easy to implement comparing to the past works. Also the proposed PFM strategy is based on the application of increasing dc

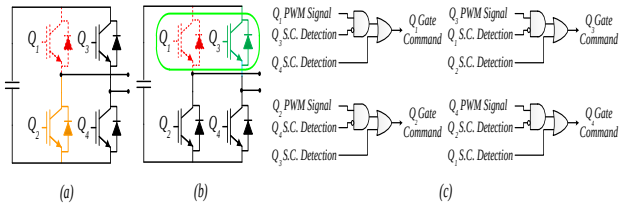

Figure 2. Structural reconfiguration strategy for a faultyHBcell (a) The short-switch fault occurs in Q_1 and the gate command for Q_2 becomes active.(b) The damaged HB cell should be bypassed by Q_1 and Q_3.(c) The proposed protection scheme for a faulty HB cell

bus utilization techniques in conjunction with the phase shifted pulse width modulation method. This strategy generates balanced grid currents during faults without adding any extra devices to the converter topology which makes this method superior to the past works. With the presented method, the converter is able to control the transmission line power flow with the remaining healthy H-bridges. The proposed short-switch fault protection scheme and the PFM strategy can extend normal operation of the SSSC and, in some cases, derate the system to prevent unexpected shutdowns.

The short-switch fault protection scheme and the principles of bypassing faulty HB cell with its own healthy switches is provided in section 2. Reconfiguration of modulation method based on adding third harmonic to the PWM reference signal, and derating the system to an intact power level is proposed in

section 3. Section 4 describes the application of the proposed strategy to a seven-level CHB converter and provides several simulation waveforms that verify the capabilities and merits of the strategy. Finally, conclusion is provided in section 5.

2. Structural reconfiguration

High-power energy conversion applications have created new demands on insulated-gate bipolar transistors (IGBTs), e.g. higher current and voltage requirements, increased power density, faster switching speeds, higher efficiencies, reliable and fast protections [17], [18]. Short-circuit fault in a fully controlled power semiconductor device needs to be detected within 10 μs to save the semiconductor devices from destruction and to avoid a shoot-through fault with the complementary device. In power converter systems, a gate drive circuit serves as an interface between the controller and the power transistors. A short circuit in an IGBT is usually detected using a hardware circuit, often with additional sensors and associate circuitries. These sensors and circuits are usually integrated in a gate driver to form a smart gate driver. Various approaches have been proposed to protect IGBTs based on the measurement of the collector current, collector-emitter voltage, gate voltage, and current rising rate [19-21]. Recently, changes in the gate voltage and the di/dt have been analyzed to identify the fault condition [17], [21]. These protection methods present a small fault detection time and are preferable to be integrated within a gate driver chip.

Generally, in most power electronics converters, one of the most significant duties of an active/smart power semiconductor gate drive is to detect the short circuit condition and consequently turning off the switch, where these functions must be performed quickly in order to maintain the switch and prevent further destructions. Most of the time this situation occurs when a complimentary device is in short circuit situation, so turning off the switch will prevent damage of the healthy device. It should be noted that preventing damage of the healthy devices needs more actions for converters in series with the transmission line. Thus, a new protective scheme which is proposed in Figure 2, can be used to improve the converter protection against short-switch faults. With this protective scheme, healthy switches will be maintained, damaged HB cell will be bypassed, and further damages will be avoided.

To explain the protective scheme operation, it can be assumed that in an HB converter, as shown in Figure 2(a), a short-switch fault occurs in Q_1, and then, the gate command for Q_2 becomes active, in this situation, Q_2's current will increase with a high rate, and also its V_{CE} will become more than normal value; subsequently, Q_2's gate driver will turn it off slowly and activate the short-circuit fault detection flag for Q_2, which means that Q_2 is in short-circuit condition. Then, Q_3 and Q_4 will be turned on and turned off respectively by logic circuitries depicted in Figure 2(c). In this way, the damaged HB cell would be bypassed by Q_1 and Q_3 (as shown in Figure 2(b)), and moreover, shoot through occurrence and sudden discharge of the dc bus capacitor will be prevented. Due to the analog circuits, the proposed protective scheme is very fast and simple.

3. Modulation reconfiguration

As mentioned previously, various methods for post-fault modulation (PFM) have been proposed with the aim of producing balanced line voltages using faultless HB cells. Although these methods can produce balanced line voltages for ac motor drives, but cannot effectively act as appropriate PFMreconfiguration solutions for applications same as SSSC, which is made up of separated converters in each phase. In addition, several methods based on redundant HB cells are also provided in the literatures reviewed in the introduction, but such solutions require complex and time-consuming steps to provide the initial charge of the dc bus capacitors in a damaged converter without any independent dc power supply in the dc buses. Moreover, embedding redundant HB cells leads to more cost, size, and weight.

During reconfiguring the converter and reducing the number of active HB cells, if the damaged HB cell can be bypassed quickly and the faultless HB cells can recover the lost power of the faulty one, the disturbance on the currents and the voltages of the converter will be transient and slight. Generally, the phase

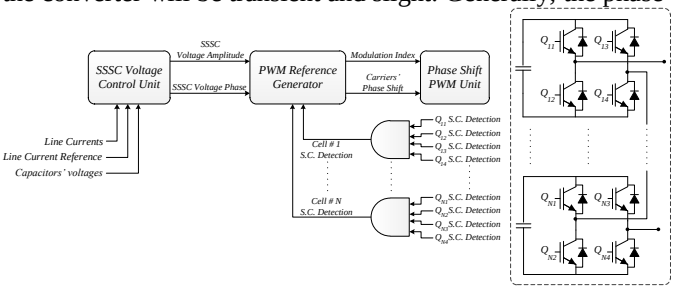

Figure 3. Control, protection, and modulation units of the short-switch fault-tolerant converter

angle of the transmission line current in an SSSC can be realized by a digital phase locked loop (PLL), which provides slow dynamics and will not be affected by mild transient disturbances; in addition, during the structural reconfiguration procedure which is proposed in this paper, the PLL remains stable, and as a result, the control system will not be disturbed.

To resolve the aforementioned problems, and realize a convenient rehabilitation, two new strategies are discussed in this section. The first is based on generating square wave voltages (SWVs) in the healthy cells of the faulty phase, and the second uses the third harmonic injection (THI) to the voltage references of the faulty phase. Both methods are executable on the same platform similar to Figure 3. The block diagram of the SSSC control and protection system are shown in Figure 3. The PWM reference generator unit receives the desired amplitude and phase angle from the main control unit, and also all the fault detection flags of the gate drivers, then, generates the carriers' phase shifts and the phase voltage references for the phase shift PWM unit during normal operation and fault situation.

3.1. Square wave voltage generation

Generating SWV is the easiest way to increase the fundamental harmonic amplitude in the output voltage of the HB converters.

If the modulation method in healthy HB cells of the faulty phase changes from sine PWM to the SWV generation, the effect of lost HB cell can be compensated by the healthy ones. In this case, the fundamental harmonic will be increased at a rate of $4/\pi$ in comparison with sine PWM [22, 23].

As the SSSC is placed in series with the transmission line, it needs just a low percentage of transmission line voltage (maximum 10%) to control the power flow [1]. Thus the injection of such a SWV has no devastating impact on the line voltage waveforms and also keeps the transmission system requirements.

Table 1. The amount of compensation for the SWV Strategy

Number of HB cells (per phase)	Recovered Voltage Percentage of the Lost HB	Recovered Voltage Percentage of the Faulty Phase	Compensation Capability
2	27.3	63.65	partial
3	54.6	84.86	partial
4	81.9	95.48	partial
5	100	100	complete

For different numbers of HB cells per phase for the SSSC, the amount of compensation for SWV strategy is shown in Table 1. Apparently, if the HB cells per phase are equal to 5 or more, the defect of lost HB cell can be compensated by the other healthy ones.

The considerable point in the performance of an SSSC in the transmission system is that the converter does not necessarily work at its rated voltage in normal operation, and the output voltage is dependent on the amount of compensation required in the transmission line. Therefore, if the maximum available output voltage of the converter be less than its rated voltage, just the transmission ability may be limited to the lower value, and the system will works properly. In this case, the transmission system can continue to its function in a different operating point. For instance, in a seven-level CHB (three HB cells per phase), under the fault condition, more than 84% of its rated phase voltage can be recoverable by using the SWV method.

The SSSC phase voltage for the faulty phase, before and after fault occurrence, for a nine-level CHB which consists of four HB cells per phase using the SWV strategy is depicted in Figure 4. In this case, short-switch fault occurs in one of the four HB cells, and the lost voltage will be recovered by the three other healthy HB cells, and the fundamental harmonic amplitude of the output voltage remains constant.

The SWV strategy can be an effective way for post-fault operation of CHB converters which have independent dc power sources to supply the dc buses of the HB cells.

The shortcomings of SWV strategy are that a wide range of high-order voltage harmonics applies to the converter transformer which increases the transformer losses and the possibility of ferroresonance phenomenon occurrence in power system, and also it can cause electromagnetic interference in communication systems. The principal privilege of the SSSC is that there is no auxiliary dc power source to provide dc voltages of the HB cells and the dc bus capacitors can be charged using the transmission line current, however, balancing the capacitor voltages, which is of great importance, cannot be established by

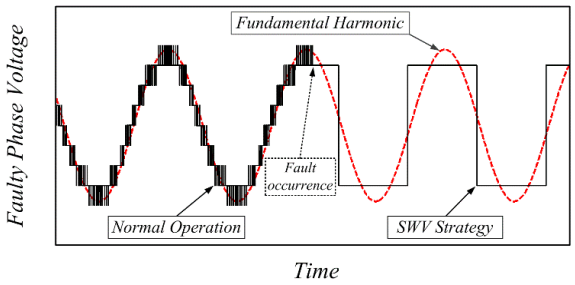

Figure 4. Square wave voltage post-fault operation strategy

using common balancing methods in parallel with the SWV strategy. Accordingly, the following strategy is proposed to modify these imperfections.

3.1. Third Harmonic Injection Strategy

The maximum modulation index of a three-phase inverter PWM system can be increased by including a third-harmonic term into the target reference waveform of each phase leg. This third-harmonic component does reduce the peak size of the envelope of each phase leg voltage. Hence the modulation index A_m can be increased beyond $A_m = 1.0$ without moving into overmodulation (i.e., the region where the reference waveform magnitudes exceed the carrier peak at various times during the fundamental cycle). Overmodulation is known to produce low-frequency baseband distortion [22, 23].

Injecting third harmonic in the phase voltage reference leads to an increase in the linear modulation range for the faulty phase. Thereby, faultless HB cells in the faulty phase can modify the effect of faulty HB cell elimination. In normal operation, N HB cells are active in each phase of the converter, so the phase voltage references and the carriers' phase shifts are as follows:

$$\begin{cases} \varphi_{PSa} = \varphi_{PSb} = \varphi_{PSc} = \dfrac{\pi}{N} \\ U_{PWMa} = A_m \,\mathrm{Sin}(\theta_a) \\ U_{PWMb} = A_m \,\mathrm{Sin}(\theta_b) \\ U_{PWMc} = A_m \,\mathrm{Sin}(\theta_c) \end{cases} \quad (1)$$

To define the appropriate sinusoidal target reference waveforms, which have been extended from equation (1) to include a third-harmonic component in the voltage production of the faulty phase, the faulty phase voltage reference equation can be written in per unit form as:

$$U_{PWMa} = A_m \,\mathrm{Sin}(\theta_a) + A_{m3} \,\mathrm{Sin}(3\theta_a) \quad (2)$$

Where A_{m3} is the third-harmonic modulation index. The maximum value of equation (2) will occur where its derivative is zero, i.e.

$$\frac{d}{dt}U_{PWMa} = A_m \mathrm{Cos}(\theta_a) + 3A_{m3}\mathrm{Cos}(3\theta_a) = 0 \quad (3)$$

For this expression to equal zero, the relation between A_m and A_{m3} is as follows:

$$A_{m3} = \frac{1}{6}A_{m3} \quad (4)$$

Under these conditions, the maximum possible modulation index A_m is

$$A_m^{\max} = \frac{2}{\sqrt{3}} = 1.1547 \quad (5)$$

This analysis shows that a 15.47% increase in modulation index can be achieved by simply injecting a one-sixth of third-harmonic into the fundamental reference waveforms. This technique is equally appropriate for naturally and regularly sampled PWM, with either a triangular or saw tooth carrier wave. Furthermore, this increase in possible modulation index is exactly that obtainable by the more elaborate method of space vector modulation which suggests increasing the modulation index by a fundamental process separate from the pulse width determination [22, 23].

According to the number of HB cells per phase, the amount of compensation using THI strategy varies, as shown in Table 2, and if the number of HB cells per phase be equal to 8 or more, the defect of lost cell can be recovered completely by other healthy cells.

As mentioned before, the point which is more important in the performance of an SSSC is to remain connected in the line even with less capability. The only effect is that the compensation performance will be reduced according to the remained healthy HB cells. By looking a glance at Table 2, it is obvious that by just having three healthy HB cells the SSSC can connected in the line even with less capability. The only effect is that the compensation performance will be reduced according to the remained healthy HB cells. By looking a glance at Table 2, it is obvious that by just having three healthy HB cells the SSSC can compensate more than 86% of its maximum compensation, which lets the SSSC to control the power flow in the line without major problem and very close to its maximum limitation in the none faulty converter.

Table 2. The amount of compensation for the THI Strategy

Number of HB cells (per phase)	Recovered Voltage Percentage of the Lost HB cell	Recovered Voltage Percentage of the Faulty Phase	Compensation Capability
2	16	57.9	partial
3	32	77.19	partial
4	47	86.8	partial
5	63	92.6	partial
6	79	96.5	partial
7	95	99.2	partial
8	100	100	complete

After the fault occurrence, N-1 number of HB cells participate in voltage production of the faulty phase, as a result, it can be concluded that the modulation index should be increased to compensate the lost part of the converter voltage. For this purpose, the new modulation index for the damaged phase should be equal to:

$$A_m^{new} = \frac{N}{N-1} \times A_m \quad (6)$$

As mention before, if the number of cells in each phase be less than 8, the lost voltage will not be fully recovered, in addition, high number of HB cells per phase, leads to high complexity of the SSSC, hence without additional restrictions, the concept is not feasible for a smaller number of HB cells.

By injecting the third harmonic with amplitude of one-sixth of the fundamental harmonic, the maximum of the fundamental can be increased by 15.47% compared to the pure sine-triangle carrier-based scheme, therefore a boundary pre-fault modulation index should be considered to avoid moving into the over-modulation region in the post-fault operation.

The boundary value for the pre-fault modulation index is equal to:

$$A_m^{boundary} = \frac{N-1}{N} \times 1.1547 \quad (7)$$

Assuming that the short-switch fault occurs in phase A, the carriers' phase shifts should be changed to new values:

$$\begin{cases} \varphi_{PSa} = \dfrac{\pi}{N-1} \\ \varphi_{PSb} = \varphi_{PSc} = \dfrac{\pi}{N} \end{cases} \quad (8)$$

Accordingly, the phase voltage references also should be changed to:

$$if\ A_m \le A_m^{boundary};$$
$$then\begin{cases} U_{PWMa} = \dfrac{N}{N-1}\left\{A_m \operatorname{Sin}(\theta_a) + \dfrac{A_m}{6}\operatorname{Sin}(3\times\theta_a)\right\} \\ U_{PWMb} = A_m \operatorname{Sin}(\theta_b) \\ U_{PWMc} = A_m \operatorname{Sin}(\theta_c) \end{cases} \quad (9)$$

In addition, there is no need to produce third harmonic voltages in the faultless phases, as for a series converter the injected voltage is small in comparison with the transmission line voltage, the added third harmonic can be neglected and does not have any devastating impact on the grid voltage.

If the pre-fault modulation index be higher than the boundary value of equation (7), the post-fault phase voltage references should be changed to:

$$if\ A_m \ge A_m^{boundary};$$
$$then\begin{cases} U_{PWMa} = 1.1547\times\left\{\operatorname{Sin}(\theta_a) + \dfrac{1}{6}\operatorname{Sin}(3\times\theta_a)\right\} \\ U_{PWMb} = \dfrac{N-1}{N}\times 1.1547\times\operatorname{Sin}(\theta_b) \\ U_{PWMc} = \dfrac{N-1}{N}\times 1.1547\times\operatorname{Sin}(\theta_c) \end{cases} \quad (10)$$

In this case, the converter cannot inject the pre-fault voltage to the transmission line and just can be connected with less output voltage, and this constraint simplifies the problem of entry to the overmodulation region and unbalanced output voltages. In order to avoid such condition, at the design stage, the upper limit for the modulation index in normal operation can be considered to be equal to the boundary value of equation (7).

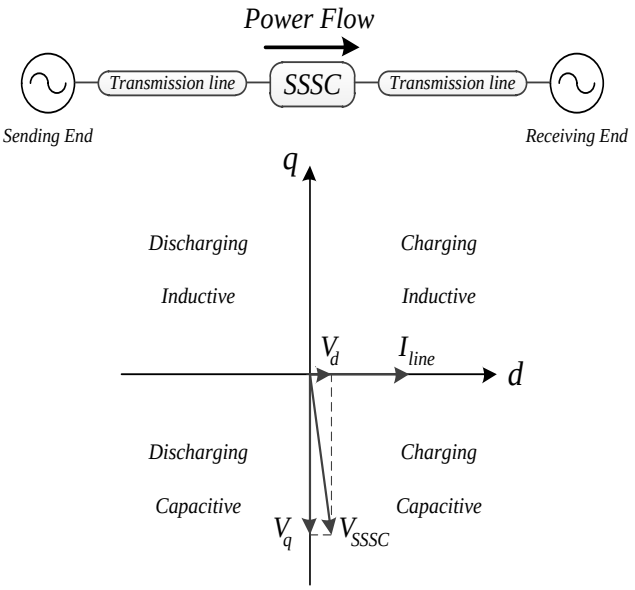

Table 3. Parameters of the simulated power system and the SSSC converter

Parameter	Value
SSSC phase voltage (at the operating point)	7.5 kV
H-bridge cells per phase	3
IGBT nominal voltage	6000 V
H-bridge dc bus voltages	4500 V
Transmission line length	150 km
Transmission line voltage	230 kV
Transmission line current	450 A
Transmission line resistance	0.089 Ω/km
Transmission line inductance	1.29 mH/km
Transmission line capacitance	7.9 nF/km
Pre-fault modulation index A_m	0.75

Figure 5. The simulated system for validating the proposed post-fault operation strategy

The noteworthy feature of the proposed THI method is that all the healthy HB cells contribute to modify the converter performance, and any changes in the main control system and its operating point are avoided. Indeed, only the modulation system will be changed, and thereby, the faultless HB cells can compensate the lost power instantly. Accordingly, the converter can continue its operation and will be able to remain active in the event of subsequent faults with the same procedure.

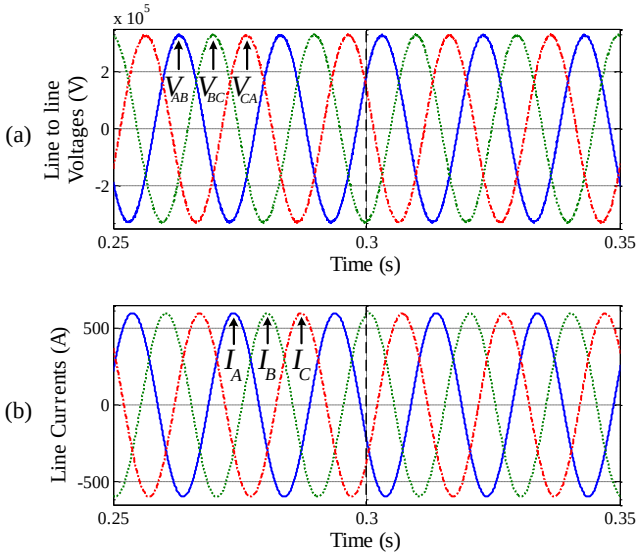

Figure 8. Transmission line phase currents, and line voltages at the receiving end.(a) Line voltages at the receiving end of the SSSC.(b) Transmission line currents.

3.3. The advantages of THI strategy compared to SWV strategy

Injecting third harmonic can be sufficient for post-fault operation and assures that the other harmonic orders are not injected to the power system, moreover, leads to a negligible temperature rise in the SSSC transformers. A significant

advantage of the THI strategy in comparison with the SWV strategy is that the capacitor voltages balancing will be realized by common balancing methods.

4. Simulation and verification

In order to verify the effectiveness of the presented post-fault operation algorithm, simulations were carried out in MATLAB/SIMULINK, where a short-switch fault in phase A of a CHB based SSSC which consists of three HB cells in each phase, occurs at time t=0.3s. The main control unit is designed so that the SSSC follows a predefined voltage command. Figure 5 illustrates the simulated system which consists of two transmission lines, and one SSSC. The parameters of the power system and the SSSC operating point are listed in Table 3. The injected voltage has a 90-degree phase shift lagging with the line current. A very small deviation from 90 degrees is provided to keep the dc bus voltages constant and compensate the inverter losses. The capacitor voltage balancing method of Saradarzadeh et al. [24] has been used, which is independent of the main control strategy, and needs only the current sign and the cells' dc bus voltages.

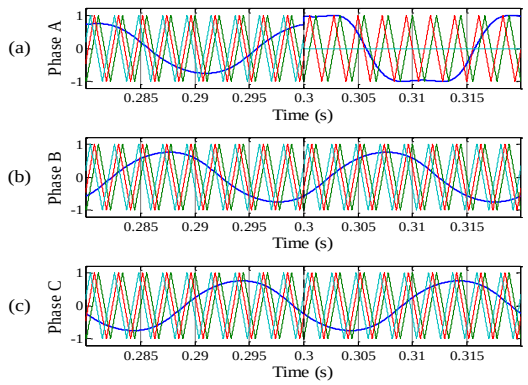

Figure 6. Carriers and references for phases A, B, and C.
(a) The carriers and the PWM reference for phase A
(b) The carriers and the PWM reference for phase B
(c) The carriers and the PWM reference for phase C

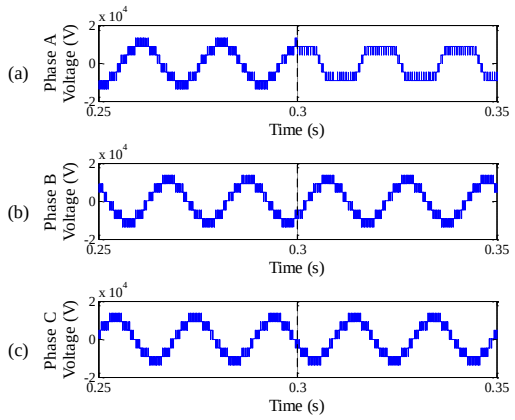

Figure 7. The SSSC phase voltages.
(a) Phase A voltage (b) Phase B voltage (c) Phase C voltage

In normal operation, three HB cells are active in each phase of the converter, so the carriers' phase shifts for phase-shift modulation method are as follows:

$$\varphi_{PSa} = \varphi_{PSb} = \varphi_{PSc} = \frac{\pi}{3}$$

The boundary value for modulation index before fault occurrence is equal to:

$$A_m^{boundary} \simeq 0.77$$

and the post-fault modulation index for the damaged phase should be equal to:

$$A_m^{new} = \frac{3}{2} \times A_m$$

Assuming that the short-switch fault occurs in phase A, the carriers' phase shifts should be changed to the new values

$$\varphi_{PSa} = \frac{\pi}{2}, \quad \varphi_{PSb} = \varphi_{PSc} = \frac{\pi}{3}$$

Accordingly, the phase voltage references also should be changed to:

$$U_{PWMa} = \frac{3}{2}\left\{ A_m \,\mathrm{Sin}(\theta_a) + \frac{A_m}{6}\,\mathrm{Sin}(3\times\theta_a) \right\}$$

Figure 6 illustrates the carriers and the PWM references for phases A, B, and C. The presented PFM reconfiguration for the faulty phase is depicted in Figure 6(a), where the carriers of the faulty phase reduces from 3 to 2, and the phase shifts between the carriers increase from 60 degrees to 90 degrees. The carriers and the PWM references of the faultless phases are depicted in Figure 6(b), (c), as well.

Figure 7 shows the SSSC phase voltages for phases A, B, and C. It can be seen from this figure that the simulation results are as expected, and the SSSC can generate balanced voltages, and reach an acceptable performance.
The transmission line currents, and line to line voltages at the receiving end of the SSSC are depicted in Figure 8, during reconfiguring the converter and reducing the number of active HB cells, the disturbances in currents and voltages of the converter are transient and negligible. Also, it can be seen from this figure that the voltages and the currents are in compliance with the system requirements.

5. Conclusion

In this work, fault tolerant operation of a CHB converter for improving the reliability and availability of large-scale power conversion as an SSSC has been described. A novel short-

switch fault protection scheme and a PFM strategy to keep the performance of a CHB based SSSC has been proposed. The fault tolerant operation has been extended to cope with the practical issue of short-switch fault in HB cells. The proposed PFM strategy is based on the application of increasing dc bus utilization techniques in conjunction with the phase shifted pulse width modulation method. With the presented PFM strategy, the converter is able to balance the three-phase grid currents and control transmission line power flow by the remaining healthy HB cells during faults. The proposed strategy can easily be implemented on CHB multilevel inverters without limitation on the number of voltage levels and adding the cost.

6. References

[1] M. Saradarzadeh, S. Farhangi, J. L. Schanen, P. O. Jeannin, and D. Frey, "Combination of power flow controller and short-circuit limiter in distribution electrical network using a cascaded H-bridge distribution-static synchronous series compensator," *IET Generation, Transmission & Distribution*, vol. 6, pp. 1121-1131, 2012.

[2] M. Saradarzadeh, S. Farhangi, J. L. Schanen, P. O. Jeannin, and D. Frey, "Application of cascaded H-bridge distribution-static synchronous series compensator in electrical distribution system power flow control," *IET Power Electron.*, vol. 5, pp. 1660-1675, 2012.

[3] Y. Yu, G. Konstantinou, B. Hredzak and V. G. Agelidis, "Operation of Cascaded H-Bridge Multilevel Converters for Large-Scale Photovoltaic Power Plants Under Bridge Failures," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7228-7236, Nov. 2015.

[4] M. Aleenejad, H. Mahmoudi and R. Ahmadi, "Unbalanced Space Vector Modulation with Fundamental Phase Shift Compensation for Faulty Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7224-7233, Oct. 2016.

[5] M. Aleenejad, H. Mahmoudi, P. Moamaei and R. Ahmadi, "A New Fault-Tolerant Strategy Based on a Modified Selective Harmonic Technique for Three-Phase Multilevel Converters With a Single Faulty Cell," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3141-3150, April 2016.

[6] S. Hayashi, T. Asakura, and Z. Sheng, "Study of machine fault diagnosis system using neural networks," in *Neural Networks, 2002. IJCNN '02. Proceedings of the 2002 International Joint Conference on*, 2002, pp. 956-961.

[7] Z. Sheng, T. Asakura, X. Xiaoli, and X. Baojie, "Fault diagnosis system for rotary machines based on fuzzy neural networks," in *Advanced Intelligent Mechatronics, 2003. AIM 2003. Proceedings. 2003 IEEE/ASME International Conference on*, 2003, pp. 199-204 vol.1.

[8] A. Bernieri, M. D. Apuzzo, L. Sansone, and M. Savastano, "A neural network approach for identification and fault diagnosis on dynamic systems," *IEEE Trans. Instrumentation and Measurement*, vol. 43, pp. 867-873, 1994.

[9] D. Eaton, J. Rama, and P. Hammond, "Neutral shift [five years of continuous operation with adjustable frequency drives]," *IEEE Ind. Appl. Magazine*, vol. 9, pp. 40-49, 2003.

[10] J. Rodriguez, P. W. Hammond, J. Pontt, R. Musalem, P. Lezana, and M. J. Escobar, "Operation of a Medium-Voltage Drive Under Faulty Conditions," *IEEE Trans. Ind. Electron.*, vol. 52, pp. 1080-1085, 2005.

[11] B. A. Welchko, T. A. Lipo, T. M. Jahns, and S. E. Schulz, "Fault tolerant three-phase AC motor drive topologies: a comparison of features, cost, and limitations," *IEEE Trans. Power Electron.*, vol. 19, pp. 1108-1116, 2004.

[12] Z. Yi, W. Xu, X. Bin, and L. Jihong, "Control Method for Cascaded H-Bridge Multilevel Inverter Failures," in *Intelligent Control and Automation, 2006. WCICA 2006. The Sixth World Congress on*, 2006, pp. 8462-8466.

[13] S. Khomfoi and L. M. Tolbert, "Fault Diagnosis and Reconfiguration for Multilevel Inverter Drive Using AI-Based Techniques," *IEEE Trans. Ind. Electron.*, vol. 54, pp. 2954-2968, 2007.

[14] P. Young-Min, L. Han-Seoung, L. Hyun-Won, J. Myung-Gil, L. Se-Hyun, and Y. Ji-Yoon, "Unbalanced three-phase control using offset-voltage for H-bridge multilevel inverter with faulty power cells," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 1790-1795.

[15] P. Barriuso, J. Dixon, P. Flores, and L. Moran, "Fault-Tolerant Reconfiguration System for Asymmetric Multilevel Converters Using Bidirectional Power Switches," *IEEE Trans. Ind. Electron.*, vol. 56, pp. 1300-1306, 2009.

[16] W. Jiang, C. Wang, Y. p. Li, and M. Wang, "Fault Detection and Remedy of Multilevel Inverter Based on BP Neural Network," in *Power and Energy Engineering Conference (APPEEC), 2012 Asia-Pacific*, 2012, pp. 1-4.

[17] W. Zhiqiang, S. Xiaojie, L. M. Tolbert, W. Fei, and B. J. Blalock, "A di/dt Feedback-Based Active Gate Driver for Smart Switching and Fast Overcurrent Protection of IGBT Modules," *IEEE Trans. Power Electron.*, vol. 29, pp. 3720-3732, 2014.

[18] B. Lu and S. K. Sharma, "A Literature Review of IGBT Fault Diagnostic and Protection Methods for Power Inverters," *IEEE Trans. Ind. Appl.*, vol. 45, pp. 1770-1777, 2009.

[19] K. Fink and S. Bernet, "Advanced Gate Drive Unit With Closed-Loop diC/dt Control," *IEEE Trans. Power Electron.*, vol. 28, pp. 2587-2595, 2013.

[20] Y. Lobsiger and J. W. Kolar, "Closed-loop IGBT gate drive featuring highly dynamic di/dt and dv/dt control," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 4754-4761.

[21] M. A. Rodriguez-Blanco, A. Claudio-Sanchez, D. Theilliol, L. G. Vela-Valdes, P. Sibaja-Teran, L. Hernandez-Gonzalez, et al., "A Failure-Detection Strategy for IGBT Based on Gate-Voltage Behavior Applied to a Motor Drive System," *IEEE Trans. Ind. Electron.*, vol. 58, pp. 1625-1633, 2011.

[22] J. W. Kelly, E. G. Strangas, and J. M. Miller, "Multiphase space vector pulse width modulation," *IEEE Trans. Energy Conversion*, vol. 18, pp. 259-264, 2003.

[23] D. G. Holmes, T. A. Lipo, Pulse width modulation for power converters: principles and practice, Vol. 18. *John Wiley & Sons*, pp. 226-250, 2003.

[24] M.Saradarzadeh, S.Farhangi, J.L.Schanen, D. Frey, P-O. Jeannin, "A Novel DC Bus Voltage Balancing of Cascaded H-Bridge Converters in D-SSSC Application," *Journal of Power Electronics*, Vol. 12, No. 4, pp. 567-577, July 2012.