A High Dynamic Range Digitally-Controlled Oscillator (DCO) for All-Digital PLL Systems

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Abstract

In this paper, a new high dynamic range Digitally-Controlled Oscillator (DCO) for All-DPLL systems is proposed. The proposed DCO is based on using a ΔΣ modulator as a Digital-to-Analog converter. Using ΔΣ DAC can provide a very high resolution (18-bit) control on the DCO. The ΔΣ DAC output is a 2-level pulse signal that needs to be filtered for cancelling the out of band shaped noise. The used ΔΣ modulator is a 4th order MASH ΔΣ modulator working with the OSR of 128 and the sampling frequency of 450MHz. the proposed DCO is used in a PLL to synthesize the frequency in the range of 1700MHz to 1800MHz for GSM-1800 application. The achieved phase noise for this PLL based synthesizer in whole the range is -115 dBc/Hz at the offset frequency of 500 kHz. The designed ADPLL including the DCO is simulated in ADS with 0.18µm CMOS technology.

Keywords: ADPLL, DCO, ΔΣ DAC, OSR, phase noise.

1. Introduction

In the recent years, the wireless communication industry has grown tremendously, leading to demand for faster and lower power consuming circuits. Because of the better properties of the digital circuits in these aspects, a great number of communication applications are moving to digital-intensive architectures [1-4].

One of the most challenging and essential blocks in any transmitter-receiver is frequency synthesizer [5-6]. This block is mainly based on phase locked-loops architecture (Figure 1). The most common PLLs used in today's wireless communication system are the fractional-N. The analog parts of the fractional-N PLL occupies large chip area and sensitive analog nodes and are difficult to design in processes with low supply voltage.

The frequency resolution demanded for a digital approach is not less issue than its analog counterparts. For example for GSM application the phase noise of -165 dBc/Hz @ 20MHz requires a DCO frequency resolution less than 1kHz for carrier of 900 MHz [14]. Typically the frequency of the DCO is tuned with

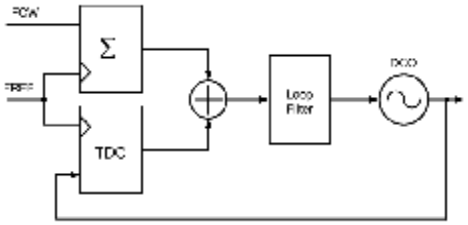

Figure 1 : All Digital PLL

varactors. In LC oscillators, two (or more) capacitor banks for coarse and fine tuning are used for digital tuning. For GHz range synthesizers, the capacitor banks with elements of the order of atto-Farads can achieve frequency resolution of the range of kHz. Although such small values can be achieved by capacitive divider networks, the sensitivity to parasitic and mismatches of these solutions limits the robustness of the design. For this limitation, a possible solution proposed in the literature by Stawsewzki et.al [2] is dithering of 3 less significant bits of the frequency control word (FCW), but because of delta-sigma data converter, the quantization noise is moved to higher frequencies where the phase noise specification is more challenging [8]. Another solution is capacitive divider network by moving part of the tuning bank of the oscillator from the tank to the source of the switching pair of the LC oscillator, which results an intrinsic shrinking used by L. Fanori et. Al [9]. This approach improves the DCO frequency resolution but is severely limited by the parasitic capacitance.

This target is reached with the solution presented in this paper where a delta-sigma digital to analog converter and a VCO is used to meet GSM specs. This paper presents a DCO design based on a scheme in Figure 2, including a ΔΣ DAC, an analog filter and an LC oscillator. In this work, circuit techniques for VCO are introduced to simplify the design and improve the DCO performance. This DCO features very high tuning range and good phase noise performance.

This paper structured as follow. An overview of the

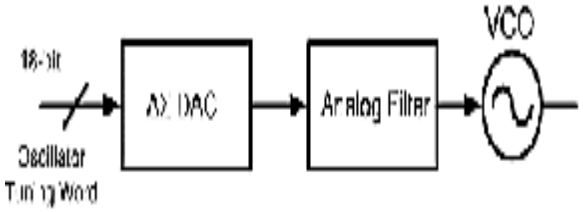

Figure 2: The signal flow diagram of the DCO

proposed DCO architecture is given in Section 2 and the DCO structure is described in the following. In Section 4, phase noise of the DCO and ADPLL is

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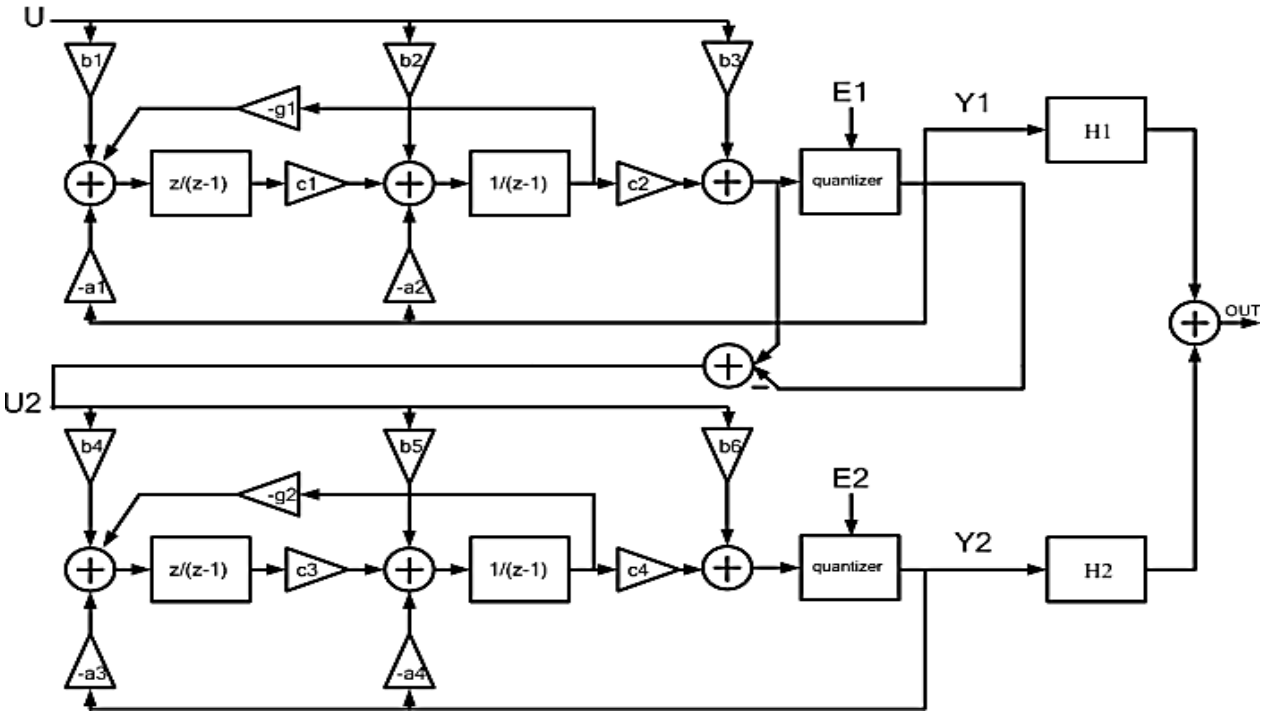

Figure 3: The 4th order 1-1 MASH ΔΣ architecture

reported. The paper ends with the conclusion in Section 5.

2. Digitally Controlled Oscillator

In this paper we present a DCO design based on a scheme in Figure 2, including a delta-sigma DAC, an analog filter and an LC oscillator [10]. In the following, the detail of the design is presented.

2.1 ΔΣ DAC System Level Design

There are many methods for performing digital-to-analog conversion. Conventional methods sample their analog inputs at the Nyquist rate. While such circuits have the advantage of simpler architectures, they also have several features that make them undesirable in large scale integrated circuits. These include requiring high precision components and stringent anti-aliasing requirements.

Through the use of oversampling, however, complexity in the analog domain can be traded off for fast and more complex digital signal processing. Because CMOS technology is better suited for fast digital circuits than precise analog circuits, high performance can be achieved using a low cost CMOS process. Furthermore, by oversampling, the quantization noise is spread out over a larger frequency [1], so that the total amount of noise in the frequency band of interest is diminished.

For GSM application, the DCO frequency resolution less than 1 kHz requires 18-bit precision for delta sigma converter. With 450 MHz sampling frequency we need 112 dB SNR and consequently forth order delta sigma modulator.

By increasing the order of the noise shaping, the NTF attenuates more quantization noise in-band and the output of the modulator becomes a more accurate representation of the input. The main difficulty with such higher order, single loop structures, however, is stability.

A solution to the stability problem is to use multi-stage noise shaping (MASH) and cascade stable first or second order single-loop structures. The output of one stage becomes the input to the next stage. The input to the next stage is simply a scaled version of the quantization error of the previous stage.

The error cancellation filters, H1 and H2 are designed such that the quantization noise from the quantizer of the first stage is cancelled. The following relations can be found from the block diagram.

$$Y_1 = STF_1.U + NTF_1.E_1 \quad (1)$$

$$Y_2 = STF_2.U_2 + NTF_2.E_2 \quad (2)$$

Where $U_2 = -E_1$ and Y_1, E_1, Y_2 and E_2 are the outputs and the power spectral densities of the first and second stage respectively. To cancels out the quantization error:

$$H_1.NTF_1 - H_2.STF_2 = 0 \quad (3)$$

From equation, we can see that one obvious choice for H1 and H2 would be: $H_1 = k.STF_2$ (4)

$$H_2 = k.NTF_1 \quad (5)$$

This work employs a 4th order multi stage noise shaping (MASH) structure to meet the SNR specification. Figure 3 shows the block diagram of the 4th order 1-1 MASH architecture. The second order Cascade of Resonators with Feedback (CRFB) topology is applied to each stage. This topology

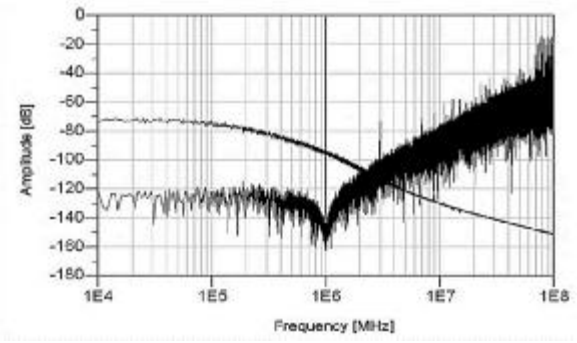

Figure 4: Spectrum of the delta sigma and its filtered output

provides an input feed forward path directly to the quantizer, which improves the modulators linearity [11].

The 18-bit digital input incoming from the digital loop filter of the ADPLL is fed to delta-sigma DAC operating at 450 MHz, which this sampling frequency can be built from the output of the ADPLL. The bandwidth of the modulator is chosen much higher than the loop bandwidth to have no impact on the performance of the overall system.

The noise transfer function of the each stage is equals to:

$$NTF = \frac{z^2 - 2z + 1}{z^2 - 1.255z + 0.4415} \quad (6)$$

The phase noise of the delta-sigma is 80 dB/Hz. A 2nd order Gm-C filter is used at the output of the delta-sigma to cancel the out of band phase noise. The output spectrum of the MASH delta sigma and its filtered output is shown in figure 4.

2.2 LC Oscillator

The VCO used in this DCO is an LC oscillator. The choice to use an LC oscillator over a ring structure has been motivated by phase noise and power consumption consideration. An LC VCO consists of three components: LC tank, tail bias transistor and cross coupled differential pair. The resonating frequency of the LC tank circuit is given by:

$$f = \frac{1}{2p\sqrt{L.C}} \quad (7)$$

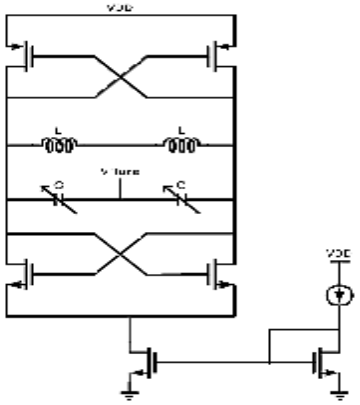

Figure 5: Differential LC tank Oscillator

A differential LC oscillator is shown in Figure 5. The tank is realized using an inductor of 1 nH with a quality factor of 50 in the middle of the frequency characteristic. The capacitance elements are back to back PMOS varactors whose sources and drain tied together. The capacitance versus control voltage (C-V) curve of one varactor is shown in Figure 6. The voltage controlled capacitance range is from 5.5 pF to 8.5 pF, which makes the oscillation frequency from 1700 MHz to 1900 MHz.

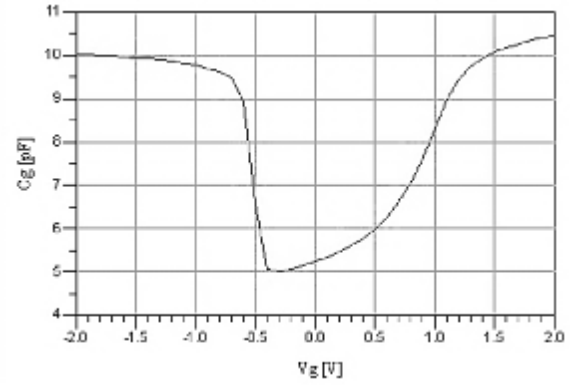

Figure 6: C-V curve of the varactor

Both Tx and Rx bands of the GSM specification in this work are supported with a single oscillator. The DCO operates in the GSM-1800 band. The DCO center frequency is 1800 MHz. The tuning range of the oscillator can be obtained from:

$$TuningRang\ \ e = \frac{w_{max} - w_{min}}{w_0} \quad (8)$$

Figure 7 shows the frequency of the DCO via its voltage tuning range.

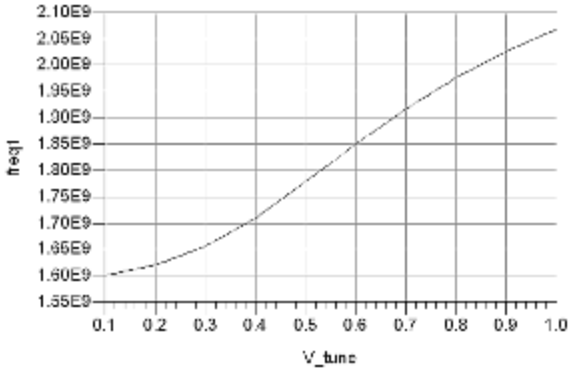

Figure 7: DCO frequency via tuning voltage

3. Simulation Results and Comparison

The proposed system has been simulated in Advanced Design System (ADS) simulator with 0.18 µm CMOS process. The optimized zeroes of the NTF for delta sigma were designed using Schreier's Delta-Sigma toolbox [14]. Figure 4 shows the Hanning-windowed of the the 1-bit output data stream spectrum of the first

stage, which is designed with CRFB topology. This delta sigma D/A converter achieved 118 dB SNR (Figure 9).

Figure 8 shows the phase noise of the presented DCO at 1800 MHz oscillation frequency. The DCO phase noise is -115 dBc/ Hz at 500 kHz offset frequency from the carrier. In comparison to the previous works, the obtained phase noise is quite desirable.

The proposed DCO is used in side of an ADPLL architecture shown in Figure 10, which implements the type II loop. Figure 11 shows the phase noise spectrum of the ADPLL with a carrier at 1.8 GHz and a loop bandwidth of 800 kHz. The reference frequency of the system is 26 MHz. In-band phase noise is -95 dBc/Hz, which dominated with time-to-digital converter and the out of band phase noise is -120 dBc/Hz at the offset frequency of 2 MHz. As presented in Figure 12, the ADPLL phase noise is under the GSM phase noise mask, which is acceptable for GSM application.

Fractional-N PLLs also use delta sigma modulator in their feedback path for extra frequency resolution and also dithering, which improves the phase noise performance of the system. Because the proposed architecture of the ADPLL is like the structure of the fractional-N PLLs, a comparison with these PLLs is presented in Table. 1

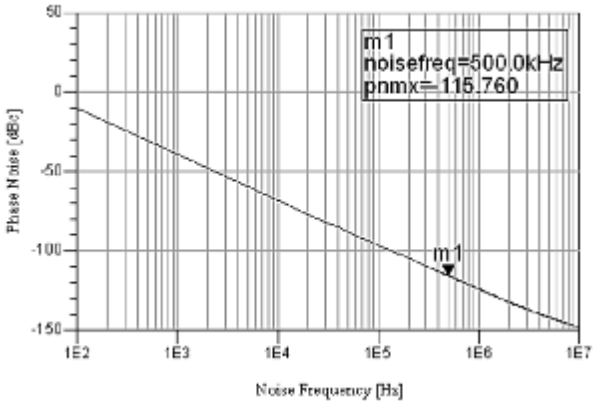

Figure 8: Phase noise of DCO

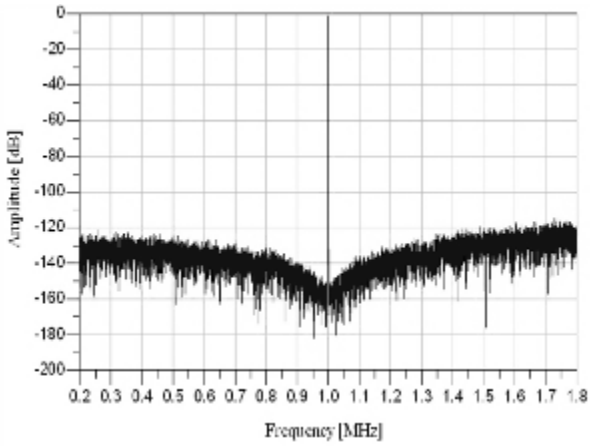

Figure 9: The output spectrum of the 4th order 1-1 MASH delta sigma

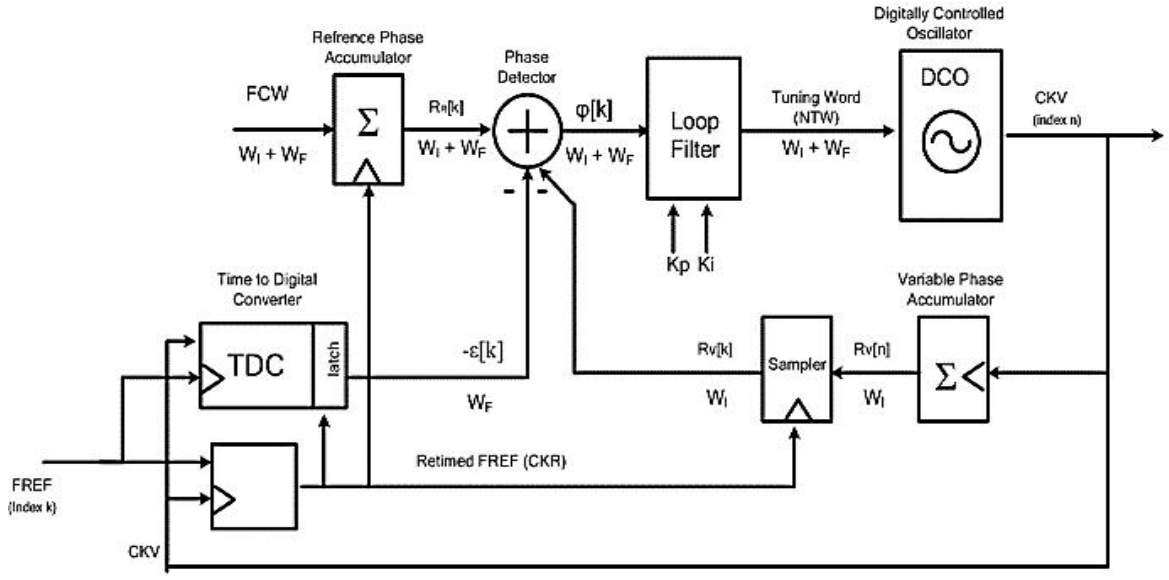

Figure 10: ADPLL Architecture

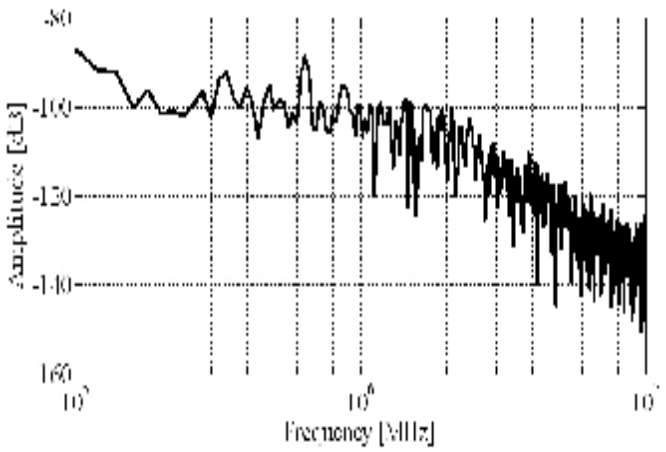

Figure 11: Phase noise of ADPLL

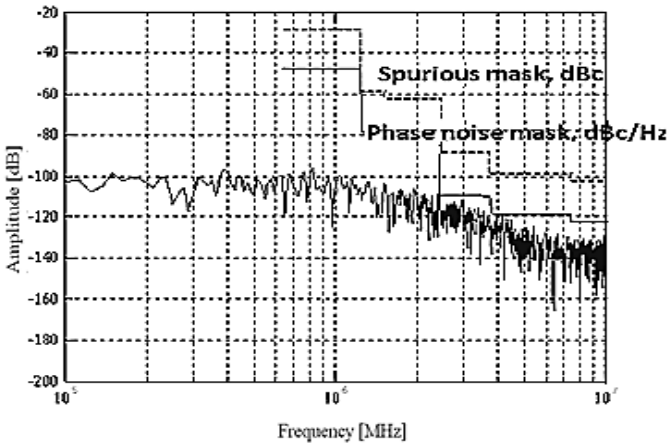

Figure 12: Phase noise of ADPLL and phase noise mask

Table 1: Performance comparison with fractional-N PLL

	[3]	[15]	[16]	[17]	This work
Technology	90	130	90	90	180
Frequency [GHz]	0.8	3.6	6	2.5	1.8
Phase noise$_{IN\text{-}band}$[dBc/Hz]	-95	-95	-95	-105	-95
Phase noise$_{out\text{-}of\text{-}band}$[dBc/Hz]	-165 dBc/Hz @20MHz	-135 dBc/Hz @3MHz	—	-115 dBc/Hz @1MHz	-120 dBc/Hz @ 2MHz
Bandwidth[kHz]	40	150	650	500	800
Implemented	*	*		*	

4. Conclusion

This paper presented an ADPLL featuring a DCO circuit for GSM application. It describes a mechanism to simplify the DCO design which is simulated in ADS. This approach allows an easier design without any additional drawbacks on the phase noise.

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