An Integrated 8-12 GHz Fractional-N Frequency Synthesizer in 90-nm CMOS

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Abstract—This work presents a fully integrated 8-12 GHz fractional-N frequency synthesizer (FNPLL) for using in communication satellites. The FNPLL implemented in a 90-nm standard CMOS technology. The simulation results demonstrate that the Voltage Controlled Oscillator (VCO) has a phase noise of -106 dBc/Hz at 1-MHz offset for a 10 GHz Local Oscillator (LO) signal, and the higher fractional spur is -55 dBc in a 10-GHz LO signal. The proposed FNPLL consumes 5.029-6.579 mW from 1.2-V power supply and has a phase noise of -70 dBc/Hz, -88 dBc/Hz and -116 dBc/Hz at 10-KHz, 100-KHz and 1-MHz offsets, respectively.

***Index Terms*—Fractional-N, Frequency Synthesizer, Phase Locked Loop, phase noise, 8-12 GHz Frequency Band**

I. INTRODUCTION

Over the last decade, single-chip integration using low-cost CMOS technology has become a major research area and the advanced CMOS processes have enabled implementation of high data rate wireless systems [1]. The demand for high data-rate and long-range wireless communication systems has propelled the rapid commercialization, which demands, use of a wideband fully-integrated Phase Locked Loop (PLL) frequency synthesizer for LO signal generation [2, 3]. Usually, the spectral purity of LO signal is a critical factor in overall transceiver performance, and the LO signal in such application are often implemented as FNPLL. Unfortunately, spurious tones are inevitable in the LO signal of FNPLLs and severely limits the performance of receiver and transmitter. Generally, spurious tone power can be reduced by increasing the linearity of key circuit blocks such as the Charge Pump (CP) and divider, restricting the choice of reference frequencies, and reducing the loop bandwidth. Unfortunately, increasing linearity tends to increase power consumption and circuit area, restricting the choice of reference frequencies reduces design flexibility, and reducing the loop bandwidth increase in-band phase noise, settling time, and loop filter size [4]. Furthermore, these methods of spurious tone reduction become less effective as CMOS circuit technology is scaled into the sub-100 nanometer regime, therefore, the spurious tone problem negatively effects on power consumption, cost, and manufacturability of wireless transceiver, and the problem gets worse as CMOS circuit technology scales with Moore's Law. However, many pervious works have been presented to design such systems. A CMOS frequency synthesizer fully compliant with multi-standard was presented in [6]. In this paper a quadrature VCO (QVCO) and SSB-mixer with inductor load has been used to realize the harmonic rejection to provide multi-standard frequency range. Apparently, the SSB-mixer can't sufficiently suppress unwanted sidebands and spurious signals. Additionally, the total four inductor in the frequency synthesizer chip will occupy large area. Another CMOS multi-standard frequency synthesizer was presented in [6]. Large reference spur and improper phase noise are the main drawbacks in this design. Additionally the author in [6] used the two QVCO as HB-VCO and LB-VCO to cover output frequency range. Apparently, the total four inductor in the frequency synthesizer chip will Occupy large area. A SiGe BiCMOS frequency synthesizer was presented in [7]. It used a classical analog frequency synthesizer with self-mixing for coverage multi-standard. Obviously, necessary condition to use the self- mixing technique in the frequency synthesizer requires to use of sharp filters. And the large area is the main drawback in this design. In this article our main focus is on investigating recently articles and using different techniques that are described in them for decreasing the total power consumption, phase noise enhancement of VCO and reference spur suppression at output LO signal. This paper is organized as follows: section 2 describes the proposed FNPLL architecture. Section 3 describes the frequency synthesizer design block. Section 4 show the simulation results and finally the conclusion will be drawn in section 5.

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I. FNPLL ARCHITECTURE

The main characteristics of a frequency synthesizer is frequency range, phase noise, spur, frequency accuracy and settling time requirements .Conventional architectures to implementation a frequency synthesizer comprises integer-N and fractional-N. Among these two architecture, integer-N architecture is easy to design. But this architecture has been fundamental shortcoming: the output channel spacing is equal to the reference frequency, limiting the loop bandwidth, reducing settling time, and needed to high division ratio divider. Instead fractional-N architecture permit a fractional relation between the channel spacing and the reference clock, that relaxing the above limitations [8]. As a consequence, a fractional-N architecture is adopted for this synthesizer. We wish to cover approximately 8-12 GHz while providing the quadrature output. Since we used two LC-VCO as HB-VCO and LB-VCO to cover the 8-10 GHz and 10-12 GHz ranges, respectively, as shown in Fig 1. The two core VCO are switched with *SW* pulse as needed. The VCO outputs followed by a prescaler and a programmable divider and the prescaler consist of two Current-Mode Logic (CML) divider. The output of CML_2 is applied to the feedback programmable divider that made of a Multi Modular Divider (MMD) and an integrated Digital Delta-Sigma Modulator (DDSM) as HK-MASH [9] with 13 bit resolution for fine channel selection. The divider output is followed by a Phase and Frequency Detector (PFD). The PFD is employed to detect the phase and frequency error between the reference frequency signal F_{ref} and the VCO divided signal F_{div} and the reference frequency for this synthesizer is set to 50-MHz. The outputs of PFD is applied to a CP and a Low Pass Filter (LPF). The 3rd order passive LPF is employed to smooth the CP output signal. Finally, the output of LPF controls oscillation frequency of the VCOs. In the following the circuit design of FNPLL blocks are presented.

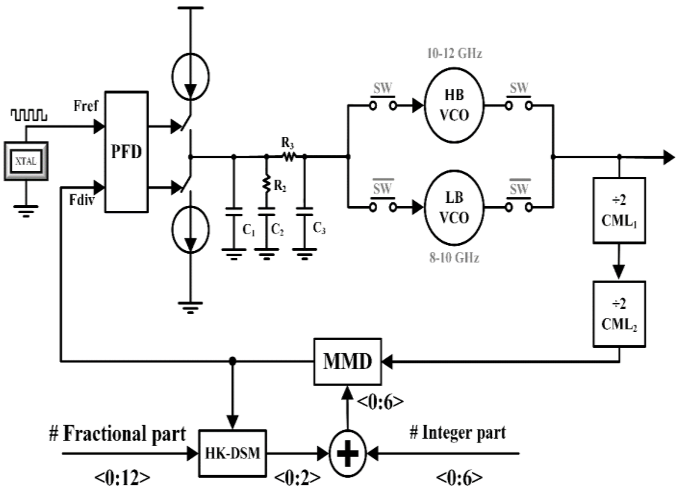


Fig 1. The proposed FNPLL

A. VCO

In order to achieve 8-12 GHz tuning range, we employed two LC-VCO. The VCO cores is based on a class-C [10] complementary NMOS and PMOS cross-coupled topology as is shown in Fig 2. This structure is thus particularly suitable to achieve low power, phase noise and high tuning range design. The LC tank are composed of an inductor and two varactors for fine frequency tuning, finally the coarse frequency tuning is employed to minimize the K_{VCO} by using 7-bit switched-capacitor network. Commonly, discrete frequency tuning performed via MOSFET switches. With this approach, the resistance and parasitic capacitor degrade the quality factor of the tank. Therefore, to overcome this problem we use the varactors in a digital manner [11] as shown in Fig 2. The current mirror drastically raises the phase noise of the VCOs. According to cadence spectre, most of the phase noise now arises from the thermal and flicker noise of M2 and M4.We used a simple modification for suppress the noise contribution of M2. As depict in Fig 2, we insert a low Pass filter between M4 and M2, suppressing the noise of M2 (and Iref). The low pass filter made of *M1*, *M3* and C_{LPF} components [8]. For filtering noise of tail transistor, we used C_2 as shown in Fig 2. The buffer used to drive prescaler, these buffers enable a transfer of The VCO signal to the prescaler without any attenuation of phase noise and signals amplitude.

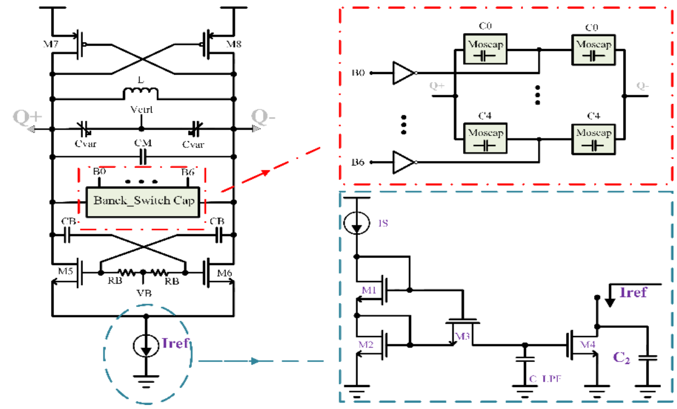


Fig 2. Schematic of the proposed VCO

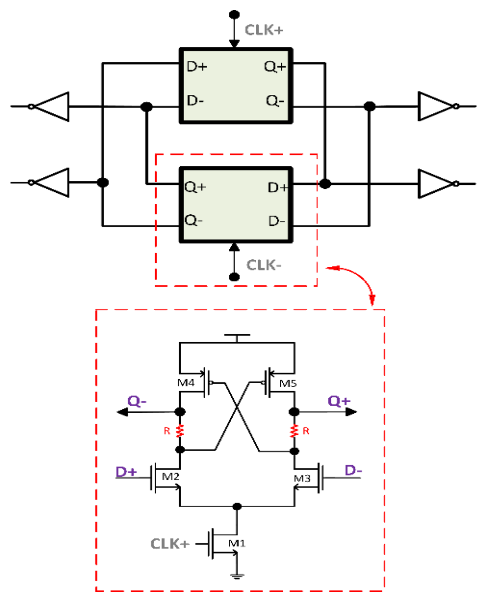


Fig 3. Schematic of the proposed analog divide-by-2

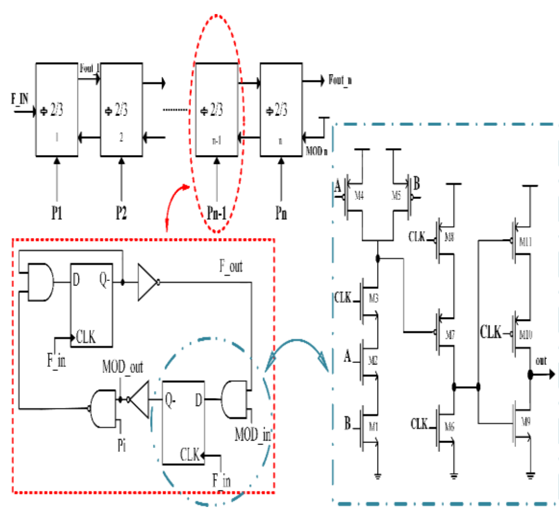


Fig 4. Schematic of the proposed MMD

B. *Prescaler and Programmable Frequency Divider*

1) *Prescaler*

The VCO output must be divided by four so as to generate quadrature output, with rail-to-rail swings available at the VCO output. In the conventional analog divider, the Differential Cascade Voltage-Switch-Logic (DCVSL) is used, but the DCVSL circuits have larger τ_{PLH} than τ_{PHL}. The favorable speed-power trade-off of the DCVSL with resistive enhancement (DCVSL-R) is presented in [12] to solve the inherent extra delay component of τ_{PLH} in DCVSL circuits, as depict in Fig 3. The resistors (R) increase the gate overdrive of PMOS load transistor. Finally it leads to getting more speed and lower power consumption at this structure. More details about this topology can be found in [12]. The CML_1 is a critical block in our frequency synthesizer and we designed this divider for operation up to 13-GHz.

2) *Programmable frequency divider*

Fig 4 illustrate the circuit of a MMD, which consist of chain of 2/3 divider cells. The division ratio for the MMD with 7-cell can be determined by the following Eq.1:

$$N=2^7+2^6.P_7+2^5.P_6+2^4.P_5+2^3.P_4+2^2.P_3+2.P_2+P_1 \qquad (1)$$

Where N is the division ration and P_i is the control bit. Since the N cells according to Eq. (1) provide division ratio from 2^N to $2^{N+1}-1$, we use 7-bits control words to cover the 127-255 division range. The divide-by-2/3 cell is a divide-by-2 divider with the option to take one extra period to the input signal when desired P_i is set to 1. The detail of the divide-by-2/3 cell and MMD can be found in [13]. The True Single-Phase Clocked (TSPC) latch [14] are used for all divide-by-2/3 cells to lessen the power consumption of the FNPLL. To enhance the operation speed of the divide- by-2/3 cell, the AND function is incorporated into the TSPC latch. The realization of the AND-TSPC latch cell is depict in Fig 4.

C. *DDSM*

The fractional division ratio is realized by the MMD together with a DDSM. The conventional structure of DDSM for FNPLL can be implemented by multi stage (MASH 2/3) of Error Feedback Modulator (EFM). The maximum sequence length MASH-DDSM for MASH 1-1-1 is 2^{N+1}, where N is the number of input bit. Recently, a novel structure for digital $\Delta\Sigma$ mash, HK-MASH has been presented [15]. In this structure a modified structure of EFM is used, just by a feedback of the output to the input of EFM with a specific gain. We employed HK-MASH 1-1-1 as 13-bit for two main reason. (1) Using HK-MASH guarantees of spurs-tone rejection of $\Delta\Sigma$ at output of fractional-tone, (2) having 13-bit avoids of complexity of structure, because the feedback gain is 1 and we need only one stage of delay (Z^{-1}). In this structure the maximum sequence length of MASH digital $\Delta\Sigma$ modulator for HK-MASH 1-1-1 is approximately 2^{3N}. Fig 5 shows the structure of a HK-MASH DDSM. The structure comprising of three cascaded of first order modified EFM. The input to each stage is the quantized error of the pervious stage. The noise cancellation network is used to eliminate the quantized error of the stages. The detail Operation of the HK-MSASH modulator is in [15].

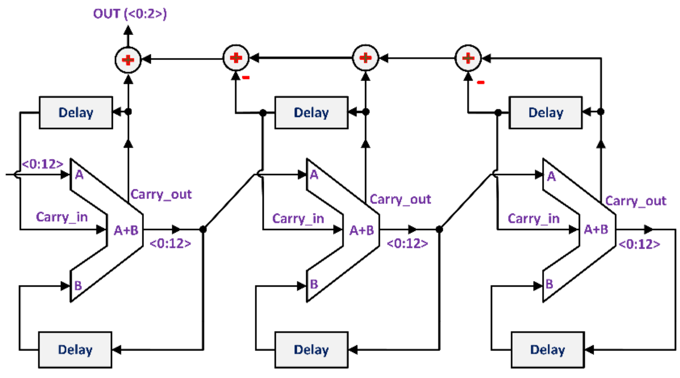


Fig 5. System level of the proposed DDSM

D. *PFD/CP*

In this structure we used the conventional static PFD. A low precision PFD has a wide dead zone (undetectable phase difference range), which results in increased jitter. The jitter caused by the large dead zone can be reduced by increasing the precision of the phase frequency detector. For avoid this problem, the delay of the RESET path was adjusted such that both *UP* pulse and *DOWN* pulse of the CP are briefly activated if the phase error is zero. This eliminates the dead zone of the PFD/CP, reducing the resulting jitter. The two current source in a CP inevitably suffer from random mismatch, and that lead to larger reference spur at LO signal. The random mismatch between the *UP* and *DOWN* current can be reduced by enlarging the current-source transistor. But larger transistor suffer from a greater amount of charge injection and clock feedthrough. We used the simple and favorable CP reported in [15]. Fig 6 illustrate the CP operation as follows: when the output voltage rises, the down current (I_{dn}) increases while the up current (I_{up}) decreases, owing to the channel-length modulation phenomenon. As the voltage increases further, eventually the *M5* enters deep triode region. The lowered device on-resistance reduces the amount of current mirrored to the output down current branch; hence it reduces the difference between I_{up} and I_{dn}. Similarly, if the CP output voltage decreases, *M9* enters the triode region. The lowered device on-resistance reduces the current mirrored to the output up current branch, and improves the up/down current matching.

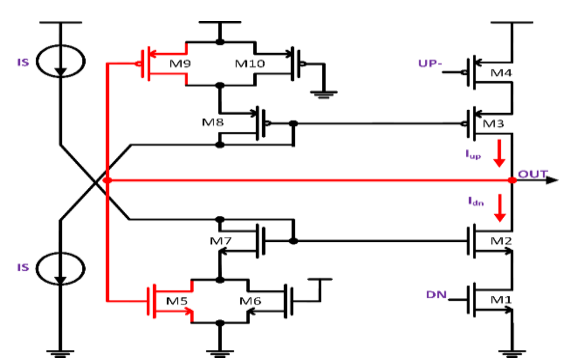


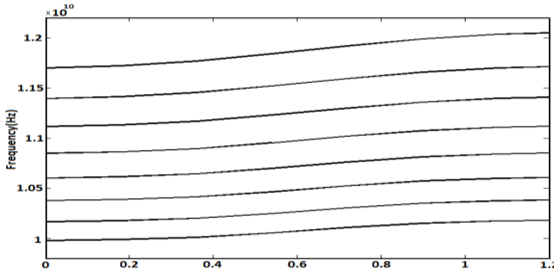
Fig 6. Schematic of the proposed CP

II. SIMULATION RESULTS

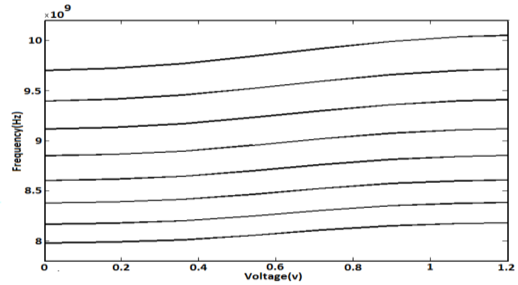
The proposed FNPLL is designed in 0.18-µm standard CMOS technology. Table 2 shows a performance summery of the FNPLL. The maximum power consumption is about 6.579 mW. In this structure we employed two LC-VCO for covering the frequency range of 8-12 GHz, as mentioned in section 2. Fig 7 shows the output frequency versus tuning voltage and digital words controlling the switched-capacitor array in simulation. The tuning range of VCO Exhibits a K_{VCO} about 300 MHz/V with a variation of less than $\pm 10\%$ over the entire tuning range. The phase noise of PFD/CP is depicted in Fig 8. Also, in Fig 9 the simulation phase noise of the VCO is depicted that the phase noise of the design is equal to -106 dBc/Hz at 1-MHz offset. In addition, the normalized phase noise of the DDSM is depicted in Fig 10. Finally, the phase noise of the proposed FNPLL is depicted in Fig 11. Fig 12 depicted simulation for the voltage control of the VCO at locked condition for 10.004-GHz frequency set-point which demonstrate that the locked time for this channel is about 150-µs. Fig 13 shows the power spectral density of the LO signal in 10.004-GHz frequency set-point. Table 2 compares the proposed synthesizer designed with recently published state-of-the-arts analog LO generation systems for wireless applications. Also the designed circuit has been tested in the worst-case (SS corner at $85°C$).

TABLE I
PERFORMANCE SUMMARY OF THE FNPLL

Parameter	simulation Value
Technology	90-nm Standard CMOS
VCO frequency range	8-12-GHz
VCO type	LC-VCO
Reference frequency	50-MHz
Step size	6 KHz (13 bit ΔΣ modulator)
Reference spur level	-55 dBm
Phase noise @ 10-KHz	-70 dBc/Hz
Phase noise @ 100-KHz	-88 dBc/Hz
Phase noise @ 1-MHz	-116 dBc/Hz
Settling time	150 µs
Supply voltage	1.2 V
power consumption	5.029-6.579 mW



(a)



(b)

Fig 7. Simulated tuning range of *7* sub-band *for (a) HB-VCO and (b) LB-VCO*

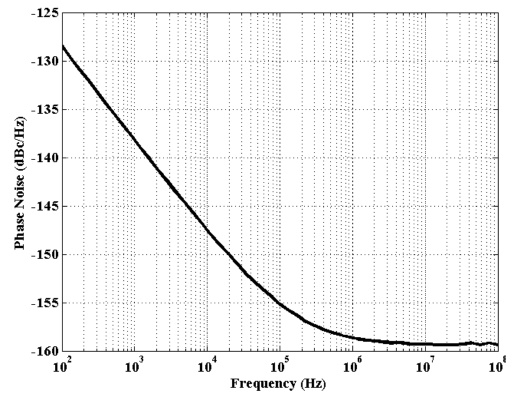


Fig 8. Phase noise of the PFD/CP

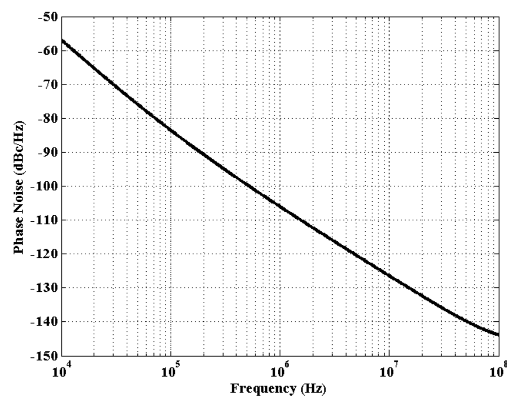


Fig 9. Simulation phase noise of the VCOs in the 10-GHz frequency set-point

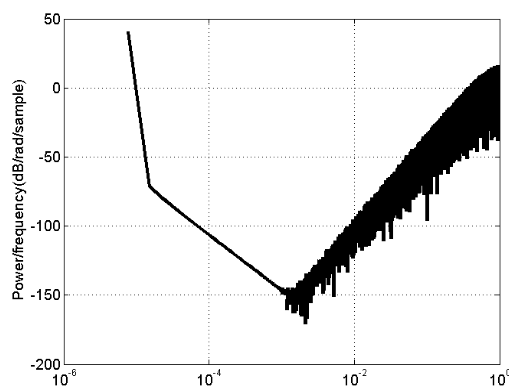


Fig 10. Normalized phase noise of the DDSM

TABLE II
. COMPARES THE PROPOSED SYNTHESIZER DESIGNED WITH RECENTLY PUBLISHED STATE-OF-THE-ARTS

Parameter	[16]	[17]	[6]	This Work
Technology	130-nm CMOS	0.25-µm SiGe	180-nm CMOS	90-nm CMOS
Frequency Range	2.158-5.133 GHz	8-12 GHz	1.78-3.05	8-12 GHz
Phase Noise @ 1-MHz	-116.8 dBc/Hz	-106 dBc/Hz	NA	-116 dBc/Hz
Power Consumption	5.14 mW	976.8 mW	9.2 mW	5.029-6.579 mW
Large Fractional Spur	-44 dBm	-64 dBm	-51 dBm	-55 dBm

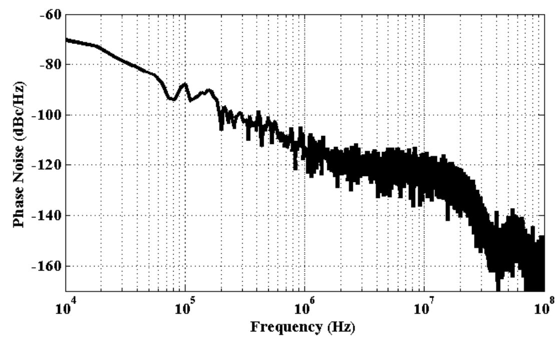


Fig 11. Total phase noise of the FNPLL

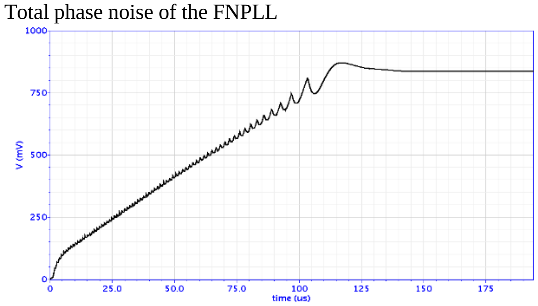


Fig 12. Control voltage during loop settling

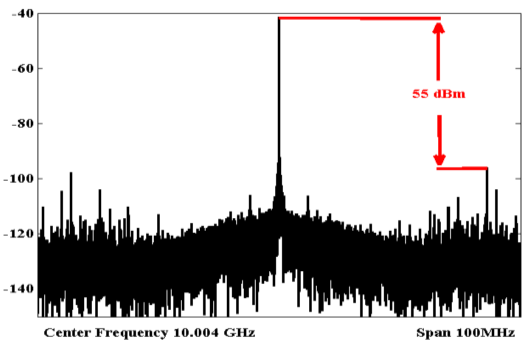


Fig 13. Spectrum of the LO signal in 10.004-GHz frequency set-point

I. CONCLUSION

An integrated FNPLL for cover the 8-12 GHz frequency range is proposed in this article. The implementation of this work has been demonstrate in 0.18-µm standard CMOS. The proposed architecture utilizes several technique to alleviate the presence of mismatch current of the CP, enhancement the phase noise of VCO. The simulation results demonstrate that the Voltage Controlled Oscillator (VCO) has a phase noise of -106 dBc/Hz at 1-MHz offset for a 10 GHz Local Oscillator (LO) signal, and the higher fractional spur is -55 dBc in a 10-GHz LO signal. The proposed FNPLL consumes 5.029-6.579 mW from 1.2-V power supply and have a phase noise of -70 dBc/Hz, -88 dBc/Hz and -116 dBc/Hz at 10-KHz, 100-KHz and 1-MHz offsets, respectively.

REFERENCES

[1] A.D. Berny, A.M. Niknejad, and R.G. Meyer, A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration, IEEE J. Solid-State Circuits 40 (4) (2005) 909-917.

[2] He, Ming, et al, 20.5 A 40nm dual-band 3-stream 802.11 a/b/g/n/ac MIMO WLAN SoC with 1.1 Gb/s over-the-air throughput, Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014, pp. 350-351.

[3] Liu, Xiaolong, et al, A 3.45–4.22 GHz PLL frequency synthesizer with constant loop bandwidth for WLAN applications, International Midwest Symposium Circuits and Systems (MWSCAS), 2014, pp. 1728-1731.

[4] Huang, Deping, et al, A frequency synthesizer with optimally coupled QVCO and harmonic-rejection SSBmixer for multi-standard wireless receiver, IEEE J. Solid-State Circuits 46 (6) (2011) 1307-1320.

[5] Huang, Fuqing, et al. "A 1.78–3.05 GHz fractional-N frequency synthesizer with power reduced multi-modulus divider." ANALOG INTEGR CIRC S, 72 (1) (2012) 97-109.

[6] Koukab, Adil, Yu Lei, and Michel J. Declercq, A GSM-GPRS/UMTS FDD-TDD/WLAN 802.11 abg multi-standard carrier generation system, IEEE J. Solid-State Circuits 41 (7) (2006) 1513-1521.

[7] B. Razavi, RF Microelectronics, second ed., Prentice Hall, 2011.

[8] Hosseini, Kaveh, and Michael Peter Kennedy, Maximum sequence length MASH digital delta–sigma modulators, IEEE Trans. Circuits Syst. I: Regul. Pap. 54 (12) (2007) 2628-2638.

[9] Mazzanti, Andrea, and Pietro Andreani, Class-C harmonic MOS VCOs, with a general result on phase noise, IEEE J. Solid-State Circuits 43 (12) (2008) 2716-2729.

[10] Osmany, S. A., et al, Integrated 22 GHz low-phase-noise VCO with digital tuning in SiGe BiCMOS technology, IEE Electron. Lett. 45 (1) (2009) 39-40.

[11] Turker, Didem Zeliha, Sunil P. Khatri, and Edgar Sánchez-Sinencio, A DCVSL delay cell for fast low power frequency synthesis applications, IEEE Trans. Circuits Syst. I: Regul. Pap. 58 (6) (2011) 1225-1238.

[12] Vaucher, Cicero S., et al. A family of low-power truly modular programmable dividers in standard 0.35-/spl mu/m CMOS technology, IEEE J. Solid-State Circuits 35 (7) (2000) 1039-1045.

[13] Yu, Xiao Peng, et al. Design and optimization of the extended true single-phase clock-based prescaler, IEEE Trans. Microw. Theory Technol. 54 (11) (2006) 3828-3835.

[14] Ti, Ching-Lung, Yao-Hong Liu, and Tsung-Hsien Lin, A 2.4-GHz fractional-N PLL with a PFD/CP linearization and an improved CP circuit, Proceedings of the IEEE International Symposium on Circuits and Systems, 2008, pp. 1728-1731.

[15] Hati, Manas Kumar, and Tarun Kanti Bhattacharyya: 'A fast automatic frequency and amplitude control LC-VCO circuit with noise filtering technique for a fractional-N PLL frequency synthesizer', Microelectronics Journal, 2016, 52: 134-146

[16] Herzel, Frank, et al. "An integrated 8-12 GHz fractional-N frequency synthesizer in SiGe BiCMOS for satellite communications." *Analog Integrated Circuits and Signal Processing* 65.1 (2010): 21-32