A wide spectral range Single-Photon Avalanche Diode implemented in 65nm standard CMOS Technology

Mohammad Azim Karami [1*], Iman Ansaripour[2]

Received: 2015/10/06 Accepted 2016/1/06

Abstract

This paper presents a wide spectral range Single-Photon Avalanche Diode (SPAD) implemented in 65nm standard CMOS (Complementary Metal Oxide Semiconductor) Technology. The wide wavelength sensitivity is achieved using the p-type substrate layer instead of using a different well implanted inside the substrate. The higher electron impact ionization coefficient in compare with the hole impact ionization coefficient results in an increase in the photon detection probability (PDP) in the larger wavelengths. Low PDP in compare with the older technologies is predictable according to the higher doping profiles of the modern deep-submicron technologies. Both the optical emission from the active region and spectral response detection is measured and analyzed in this paper.

Keywords: Single-photon avalanche Diode (SPAD), 65nm CMOS

Introduction

Quanta Image Sensors are introduced as the next generation of image sensors for the visible light imaging in the semiconductor industry [1]. A quanta image sensor stores the location and the time of each photon detection at different pixels with picosecond timing resolution, and forms the final image regarding the collection of each single-photon [2]. While conventional image sensors such as Charge Coupled Device (CCDs), and Active Pixel Sensors (APS) count the number of impinging photons in a constant time frame and store the total photon numbers in the time frame, quanta image sensors need the sensitivity of single-photon with low jitter performance to record each photon details [3]. Single-Photon Avalanche Diodes (SPADs) being made in CMOS (Complementary Metal Oxide Semiconductor) technologies are among the main candidates to make the quanta image sensor pixels [4].

Several SPADs are realized in standard and imaging CMOS technologies in 0.8µm [5], 0.35µm [6], 180nm [7], 130nm [8], 90nm [9, 10], and 65nm [11] technology nodes. While the industry pushes the SPAD production in the state of the art scaled technologies, to realize smaller pixels for higher spatial resolution cameras, designing and implementation of SPADs in scaled technologies are faced with new challenges. Higher doping profiles present in the modern CMOS technologies to compensate the Metal Oxide Semiconductor (MOS) threshold voltages have challenged the implementation of SPADs in deep-submicron technologies [12]. The use of higher doping profiles results in the reduction of the photodiode depletion width which would limits the number of photon collection in the space charge region. Moreover the thinner depletion regions causes the observation of higher band to band tunneling (BTBT) current which increases the Dark Count Rate (DCR) noise of the SPAD [13]. The DCR factor in single-photon detectors which is defined as the number of spurious pulses detected in complete dark is equivalent to the dark current in conventional photodetectors.

SPADs are characterized by DCR, Photon detection Probability (PDP), and timing resolution parameters such as timing uncertainty response (Jitter), afterpulsing probability, and the dead-time (the time which is needed for the SPAD capacitor charging) [14].

This paper evaluates the PDP response of the SPAD implemented in [15]. The PDP measurement setup is described while the PDP response is compared with similar works. The main characteristics of the PDP response are analyzed.

Implemented structure:

A SPAD consists of an active region pn junction, which generates electron-hole pairs by the photon absorption, and a guard ring surrounding

1 .***** Department of Electrical Engineering
Iran University of Science and Technology, Tehran, Iran.
Corresponding author: karami@iust.ac.ir
2.Department of Electrical Engineering
Iran University of Science and Technology, Tehran, Iran.

the active region. The guard ring is formed from lower doped wells to decrease the electric field strength surrounding the active region. With the absence of guard ring, the electric field strength would be higher on the edges of the active region and it would result in premature edge breakdown (PEB). PEB occurs when the diode breakdown occurs in the edges of the diode instead of the whole active region breakdown which needs a uniform electric field distribution in the whole active area.

SPADs are biased after the breakdown voltage in the so-called Geiger mode of operation, where a single-photon absorption creates an electron hole pair which leads to the impact ionization and avalanche current due to the high electric field. The avalanche is quenched by readout circuits and SPAD is recharged again to detect the next photon arrival. The realization of SPADs in deep-submicron technologies has become more difficult due to the Shallow Trench Isolations (STI) presence which has some accumulated charge in the oxide part [16]. Moreover, higher doping profiles and shallow wells make the SPAD realization in deep-submicron technologies more difficult.

Fig. 1. Shows the cross-section of the SPAD characterized in this paper. The SPAD consists of a n+p substrate junction and n-wells are used as the guard ring to suppress PEB.

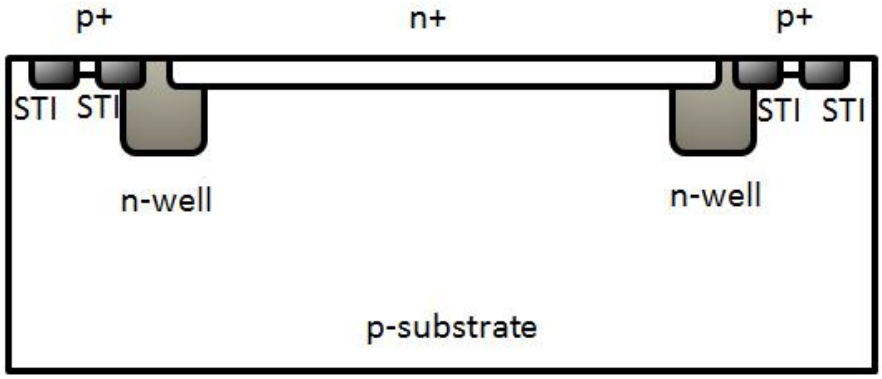

Fig. 1. SPAD cross section using n+p substrate junction as the active region and photosensitive part, and n-well as the guard ring.

Fig. 2. shows the SPAD photomicrograph with the active region in the center and the guard ring surrounding the active region. SPADs are normally implemented in circular structures to reduce the electric field strength on the edges, but the use of circular structure was restricted in 65nm CMOS technology.

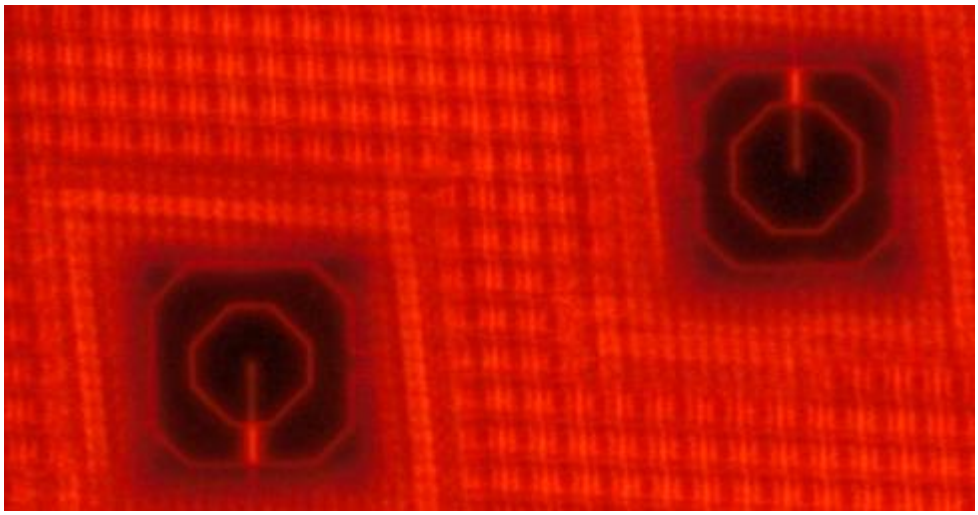

Fig. 2. SPAD photomicrograph consisting of the central octagonal part as the photosensitive part and the surrounding guard ring.

Fig. 3, shows the photoluminescence emission of the implemented SPAD which is a sign of the guard ring efficiency. Since the light emission is from the central part of the SPAD and not from the guard ring parts, it can be concluded that more electric field is present in the central part and PEB prevention. In the case of PEB, light emission is observed from the guard ring part instead of the active region [17].

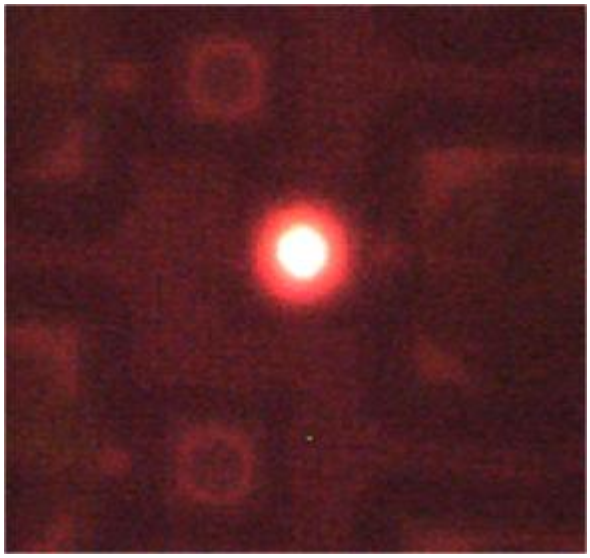

Fig. 3. The light emission from the active region of SPAD which is a sign of guard ring efficiency**.**

Photon Detection Probability (PDP)

We have characterized electrical parameters of the SPAD in [15] including: DCR (61 kHz at V_e=0.13V at 293K temperature) and the breakdown voltage of 9.5V at room temperature. It should be noted that V_e is the excess bias voltage which is the amount of additional voltage more than the measured breakdown voltage, provided to reverse bias the SPAD in Geiger mode of operation.

The PDP measurement setup which is shown in Fig. 4, consists of a monochromator which produces tunable wavelength light, harmonic canceling filter which filters the harmonics in the output light produced by the monochromator. Moreover a density filter is used to make sure of the realization of single-photon level of light. Low light level is entered to an integration sphere with a reference Metal Semiconductor Metal (MSM) photodetector and the SPAD to measure the SPAD photon count output in comparison with the reference photodetector.

The integration sphere guarantees that the number of impinging photons on the reference photodetector and the SPAD are equal. For the PDP calculation, the number of pulses counted by the SPAD (where each pulse represents a single-photon detection) are subtracted by the DCR and divided by the number of photons counted by the reference detector with near unity quantum efficiency at the same wavelength.

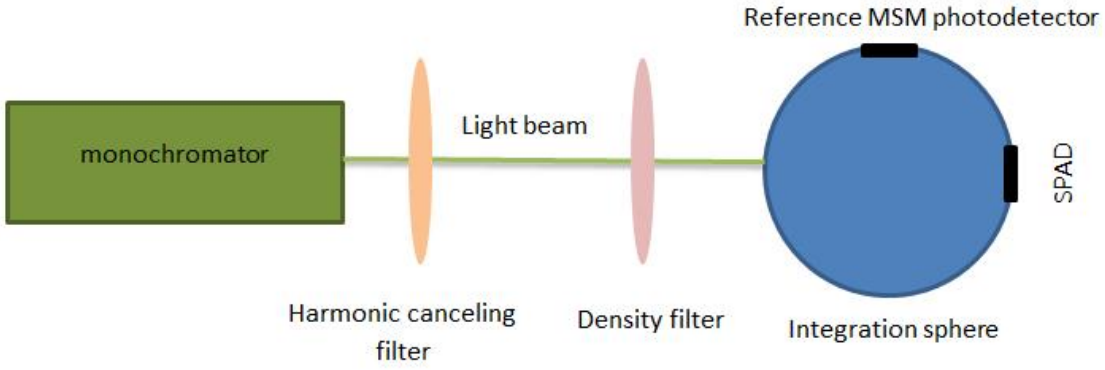

Fig. 4. PDP measurement setup consisting of a monochromator, harmonic canceling and density filters and the integration sphere.

Fig. 5. shows the PDP result of the realized SPAD obtained by using the above measurement setup. The PDP response is compared with a similar SPAD made on the same CMOS technology [11].

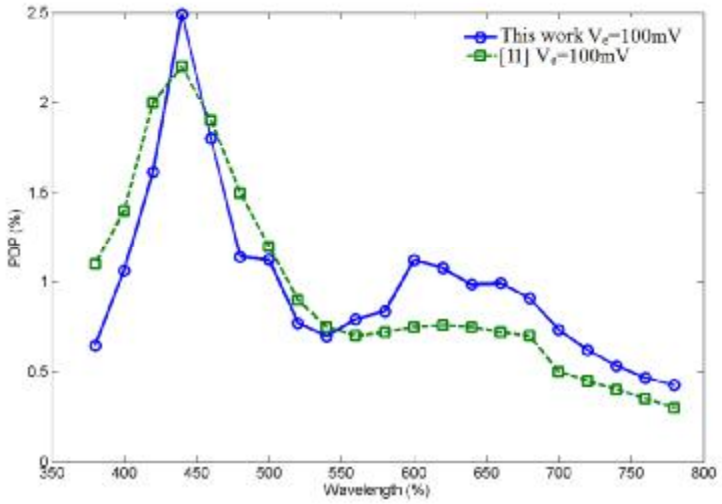

Fig. 5. PDP response of the SPAD and [11] at different wavelengths.

Discussion:

PDP is calculated using the following equation [18]:

$$PDP(l) = P_b(l).QE(l) \qquad (1)$$

Where $P_b(\lambda)$ is the breakdown probability at a certain wavelength (λ) and $QE(\lambda)$ is the quantum efficiency at the certain wavelength (λ).The equation shows that PDP is a function of both the quantum efficiency of the device and the probability of the carrier (electron or hole) to initiate an avalanche.

Different regions where electron-hole pairs are generated by the photon absorption and can contribute to the PDP are shown in Fig. 6. It is assumed that the photon absorption only occurs in the active region and the guard rings are covered with metal or thick poly layers which reduce the light penetration to the silicon substrate.

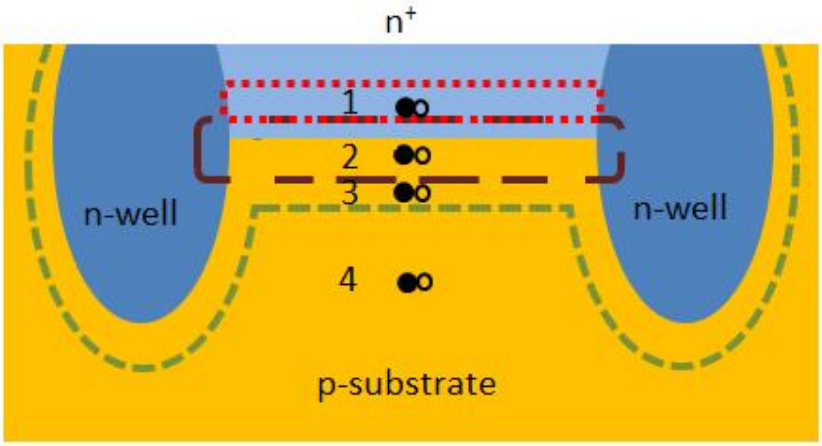

Fig. 6. Different regions of photon absorption which contribute to the PDP formation

.

Holes in n+ (region 1) can diffuse from the n+ to the junction after the absorbed light generates an electron-hole pair, possibly triggering an avalanche. Considering region 2 in Fig. 6, generated electrons or holes in the multiplication region (The region which has the electric field more than critical electric field of the semiconductor to cause impact ionization) may trigger an avalanche. Moreover, generated electrons by absorbed light in the depletion region inside p-substrate (region 3) move to the junction and may trigger an avalanche. Finally the electrons outside the depletion region inside the p-substrate (region 4) can diffuse to the depletion region and then advance to the multiplication region and create an avalanche. It should be noted that region 1 and region 4 are limited by the minority carrier diffusion length, and the carrier in these regions can create an avalanche with a delay for reaching to the multiplication region.

Since the impact ionization coefficient of holes is lower than the impact ionization coefficient of electrons in silicon [12], higher PDP is observed in the red and near-infrared (NIR) region in compare with [11]. Hence, the higher probability of electrons which are absorbed deep in the substrate, to create an avalanche results in a wide spectral range observation.

Meanwhile the PDP of the SPAD presented in this work is lower than [11] at 360nm wavelength due to the lower impact ionization coefficient of holes which can create the avalanche from n+ region. Furthermore, the maximum PDP which occurs at 440nm is higher in this work due to the higher thickness of depletion region in compare with [11].

Conclusions:

In this paper the optical response of a SPAD designed and implemented in 65nm standard CMOS technology is characterized. While the light emission from SPAD shows the guard ring efficiency, below 3 % PDP is observed due to the high doping profiles in deep-submicron technologies. The SPAD presented in this paper is benefited from wide spectral response due to using the substrate itself as a part of depletion region and preventing to restrict the depletion layer to an implanted doping well. Higher impact ionization coefficient of electrons results in higher PDPs in read and NIR part of the PDP.

Acknowledgment:
The SPAD chip realization is performed under the supervision of Prof. E. Charbon in Technical University of Delft, the Netherlands.

References

[1] Fossum, Eric. "The quanta image sensor (QIS): concepts and challenges." InImaging Systems and Applications, p. JTuE1. Optical Society of America, 2011.

[2] Ma, Jiaju, and Eric R. Fossum. "A Pump-Gate Jot Device With High Conversion Gain for a Quanta Image Sensor." Electron Devices Society, IEEE Journal of the 3, no. 2 (2015): 73-77.

[3] Masoodian, Saleh, Yue Song, Donald Hondongwa, Jiaju Ma, Kofi Odame, and Eric R. Fossum. "Early research progress on quanta image sensors." In Proc. Int. Image Sensor Workshop, Snowbird, UT, USA. 2013.

[4] Teranishi, Nobukazu. "Required conditions for photon-counting image sensors."Electron Devices, IEEE Transactions on 59, no. 8 (2012): 2199-2205.

[5] Niclass, Cristiano, Alexis Rochas, Pierre-André Besse, and Edoardo Charbon. "Design and characterization of a CMOS 3-D image sensor based on single photon avalanche diodes." Solid-State Circuits, IEEE Journal of 40, no. 9 (2005): 1847-1854.

[6] Carrara, Lucio, Cristiano Niclass, Noémy Scheidegger, Herbert Shea, and Edoardo Charbon. "A gamma, x-ray and high energy proton radiation-tolerant CIS for space applications." In Solid-State Circuits Conference-Digest of Technical Papers, 2009. ISSCC 2009. IEEE International, pp. 40-41. IEEE, 2009.

[7] Leitner, Thomas, Amos Feiningstein, Renato Turchetta, Rebecca Coath, Steven Chick, Gil Visokolov, Vitali Savuskan et al. "Measurements and simulations of low dark count rate single photon avalanche diode device in a low voltage 180-nm CMOS image sensor technology." Electron Devices, IEEE Transactions on 60, no. 6 (2013): 1982-1988.

[8] Richardson, Justin, Richard Walker, Lindsay Grant, David Stoppa, Fausto Borghetti, Edoardo Charbon, Marek Gersbach, and Robert K. Henderson. "A 32× 32 50ps resolution 10 bit time to digital converter array in 130nm CMOS for time correlated imaging." In Custom Integrated Circuits Conference, 2009. CICC'09. IEEE, pp. 77-80. IEEE, 2009.

[9] Henderson, Robert K., Eric AG Webster, Richard Walker, Justin Richardson, and Lindsay Grant. "A 3× 3, 5µm pitch, 3-transistor single photon avalanche diode array with integrated 11V bias generation in 90nm CMOS technology." InElectron Devices Meeting (IEDM), 2010 IEEE International, pp. 14-2. IEEE, 2010.

[10] Karami, Mohammad Azim, Marek Gersbach, Hyung-June Yoon, and Edoardo Charbon. "A new single-photon avalanche diode in 90nm standard CMOS technology." Optics express 18, no. 21 (2010): 22158-22166.

[11] Charbon, Edoardo, Hyung-June Yoon, and Yuki Maruyama. "A Geiger mode APD fabricated in standard 65nm CMOS technology." In Electron Devices Meeting (IEDM), 2013 IEEE International, pp. 27-5. IEEE, 2013.

[12] Taur, Yuan, and Tak H. Ning. Fundamentals of modern VLSI devices. Cambridge university press, 2009.

[13] Webster, Eric AG, and Robert K. Henderson. "A TCAD and spectroscopy study of dark count mechanisms in single-photon avalanche diodes." Electron Devices, IEEE Transactions on 60, no. 12 (2013): 4014-4019.

[14] Cova, S., M. Ghioni, A. Lotito, I. Rech, and F. Zappa. "Evolution and prospects for single-photon avalanche diodes and quenching circuits." Journal of Modern Optics 51, no. 9-10 (2004): 1267-1288.

[15] Karami, Mohammad Azim, Hyung-June Yoon, and Edoardo Charbon. "Single-Photon Avalanche Diodes in sub-100nm Standard CMOS Technologies." InProc. Intl. Image Sensor Workshop (IISW), no. EPFL-CONF-178147. 2011.

[16] Finkelstein, Hod, Mark J. Hsu, and Sadik C. Esener. "STI-bounded single-photon avalanche diode in a deep-submicrometer CMOS technology." Electron Device Letters, IEEE 27, no. 11 (2006): 887-889.

[17] Gersbach, Marek, Justin Richardson, Eric Mazaleyrat, Stephane Hardillier, Cristiano Niclass, Robert Henderson, Lindsay Grant, and Edoardo Charbon. "A low-noise single-photon detector implemented in a 130nm CMOS imaging process." Solid-State Electronics 53, no. 7 (2009): 803-808.

[18] Pancheri, Lucio, David Stoppa, and Gian-Franco Dalla Betta. "Characterization and Modeling of Breakdown Probability in Sub-Micrometer CMOS SPADs."Selected Topics in Quantum Electronics, IEEE Journal of 20, no. 6 (2014): 328-335.